AN3095
Application note

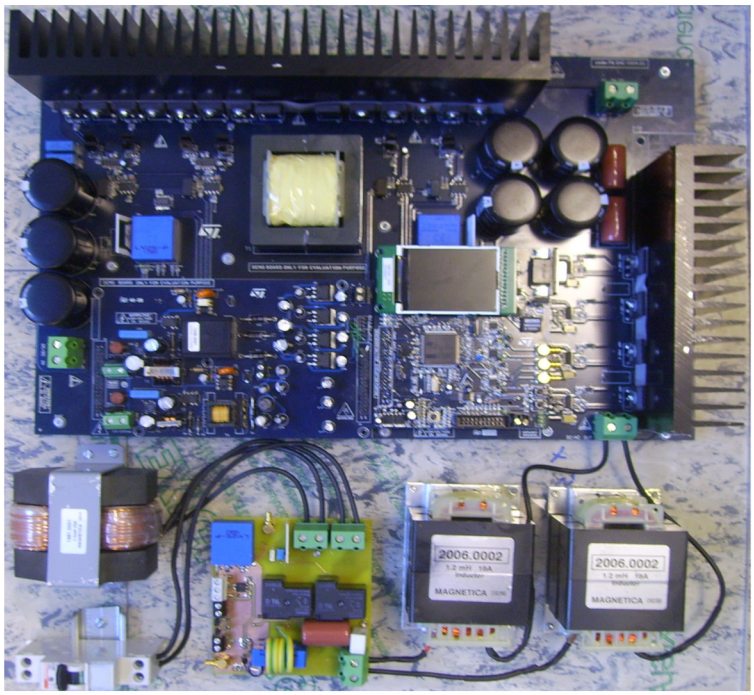
STEVAL-ISV002V1, STEVAL-ISV002V2 3 kW grid-connected PV system, based on the STM32F103xx

Introduction

The STEVAL-ISV002V2 demonstration board is the same as the STEVAL-ISV002V1, but assembled in a metal suitcase. In recent years, the interest in photovoltaic (PV) applications has grown exponentially. As PV systems need an electronic interface to be connected to the grid or standalone loads, the PV market has started appealing to many power electronics manufacturers. Improvements in design, technology and manufacturing of PV inverters, as well as cost reduction and high efficiency, are always the main objectives, [see *References 1*, *2*].

This application note describes the development and evaluation of a conversion system for PV applications with the target of achieving a significant reduction in production costs and high efficiency. It consists of a high frequency isolated input power section performing DC-DC conversion and an inverter section capable of delivering sinusoidal current of 50 Hz to the grid. The system operates with input voltages in the range of 200 V to 400 V and is tied to the grid at 230 Vrms, 50 Hz, through an LCL filter. Other peculiar characteristics of the proposed converter are the integration level, decoupled active and reactive power control and flexibility towards the source. A prototype has been realized and a fully digital control algorithm, including power management for grid-connected operation and an MPPT (maximum power point tracking) algorithm, has been implemented on a dedicated control board, equipped with a latest generation 32-bit (STM32F103xx) microprocessor.

Figure 1. 3 kW PV system image



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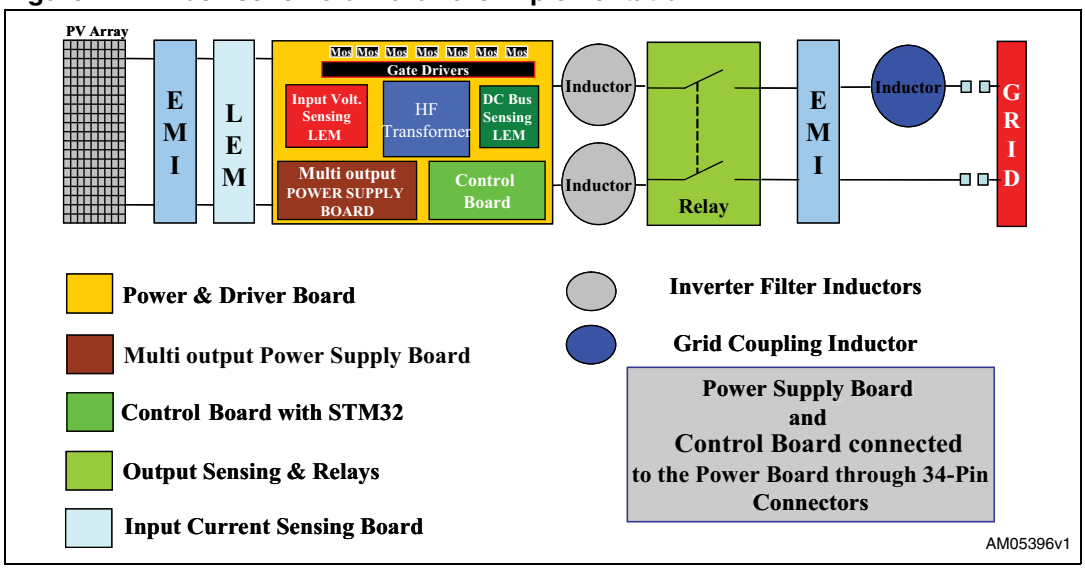
1 System description

A general description of the system is shown in *Figure 2* with a block scheme representing hardware implementation.

Figure 2. Block scheme of hardware implementation



It consists of 5 boards as listed below:

- Main power board
- Multi-output power supply board
- Control and signal conditioning board
- Output sensing and relay board
- Input current sensing board.

The system may be completed by adding two additional boards with input and output EMI filters which, at the moment, are not included in the final prototype.

The main power board is a dual-stage converter using DC-DC to adapt voltage levels and impedance from the PV array and a sinusoidal PWM DC-AC to perform grid connection at 230 Vrms and 50 Hz, [see *References 3*]. Gate driving circuitry, input and output voltage sensors of the DC-DC converter, as well as high frequency (HF) transformers, are also placed on the power board. The principle reason for using a HF transformer is the galvanic isolation provided between the PV module and the grid, to minimize the risk of hazardous operations on the PV side caused by a fault on the grid side; voltage step-up and also interruption of the resonance path formed by the parasitic capacitances to ground of the PV array and the inductance of the LCL filter. Another advantage is the elimination of high common mode currents allowing the use of unipolar pulse-width modulation for the inverter with a consequent reduction in current harmonic content compared to bipolar pulse-width modulation, [see *References 4*, *5*].

Both the multi-output power supply board and control board are connected to the main power board by means of a 34-pin connector. In this way, the connection/disconnection of the ancillary boards is very easy and allows the separation of debug and characterization.

The output sensing and relays board was realized to interface the power system and the grid. This task is accomplished with the implementation of a proper control algorithm which requires both grid-current and grid-voltage sensing. For this reason, the board is equipped with current and voltage Hall effect sensors. Two relays, controlled by an I/O of the microcontroller, are also placed on the same PCB to interrupt/connect phase and neutral of the system to phase and neutral of the grid. Moreover, this board is provided with two-way connectors for electrical wiring of the LCL filter to the main power board.

The multi-output power supply board implements two independent offline flyback converters, with wide input voltage range, based on VIPER technology, to generate the following output voltages:

- +5 V to supply DC-DC converter gate drivers
- +5 V to supply DC-AC converter gate drivers
- +5 V to supply the microcontroller
- +/-15 V for LEM sensors supply
- 24 V for relays supply

The main advantage of an offline solution is the availability of a power supply for circuits dedicated to communication and data transfer even at night or in the case of weak PV field energy production. The price to pay for such an advantage is higher power consumption during standby mode of the main power unit.

The specifications in *Table 1* for the PV system are used as inputs for the design of the boards mentioned above. All parameters are assumed to be equal to their nominal value if not otherwise stated.

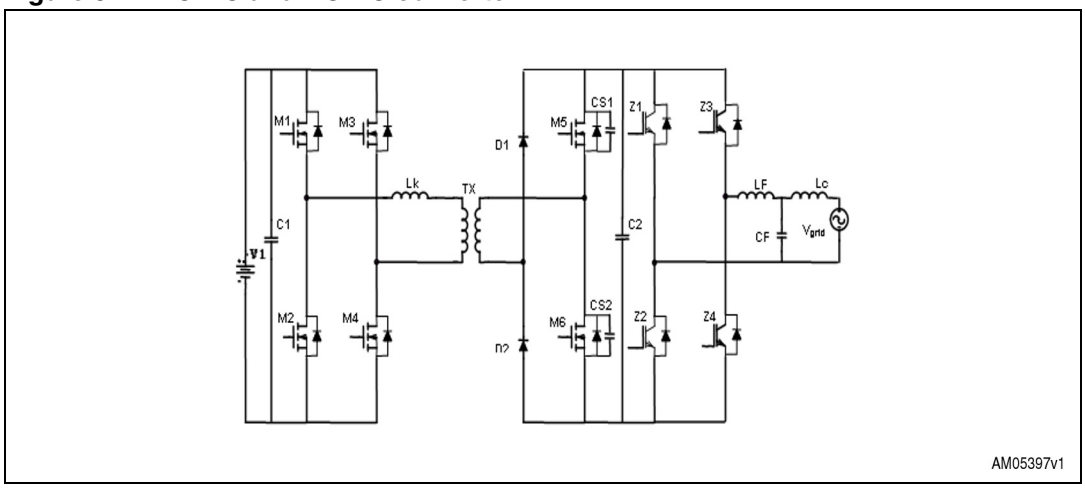
Table 1. System specifications

Specification	Value
DC-DC input voltage	200 V - 400 V
DC-DC output voltage	450 V
DC-AC output voltage	230 Vac
Nominal output power	3 kW
DC-AC switching frequency	17 kHz
DC-DC switching frequency	35 kHz
Transformer turns ratio	1.2
Grid voltage	230 Vrms +/- 20 %
Grid frequency	50 Hz
Power factor above 10 % rated power	>0.9
THD@ full load	<5 %

2 DC-DC converter

The dual-stage inverter for grid-connected applications includes a DC-DC converter to amplify the voltage and a DC-AC inverter to control the current injected into the grid.

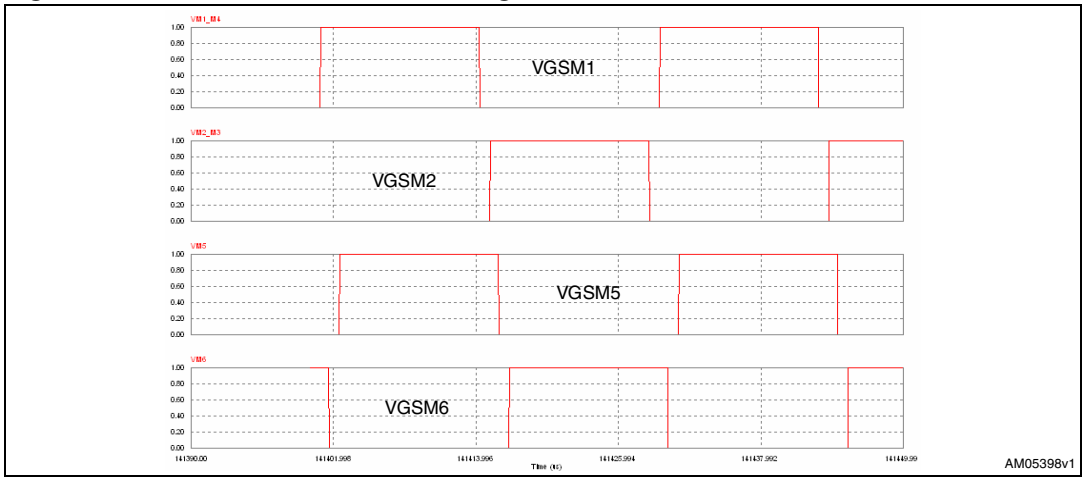
Figure 3. DC-DC and DC-AC converter



The DC-DC converter is depicted in *Figure 3* together with the DC-AC converter and LCL filter. The converter consists of an input capacitor, C1, six switches, M1 - M6, six freewheeling diodes, two rectifier diodes, D1 and D2, a HF transformer with turns ratio equal to 1.2 and a DC link capacitor C2.

The transformer provides voltage isolation between the PV array and the grid, improving overall system safety. Its leakage inductance is used as a power transfer element, eliminating device overvoltage problems and the need for snubber circuits. Proper phase-shift control between input bridge legs (M1-M4) and active rectifier legs (M5-M6) allows transformer current shaping, therefore achieving ZCZVS for all the power devices, as well as voltage step-up. The adopted phase-shift modulation is shown *Figure 4*.

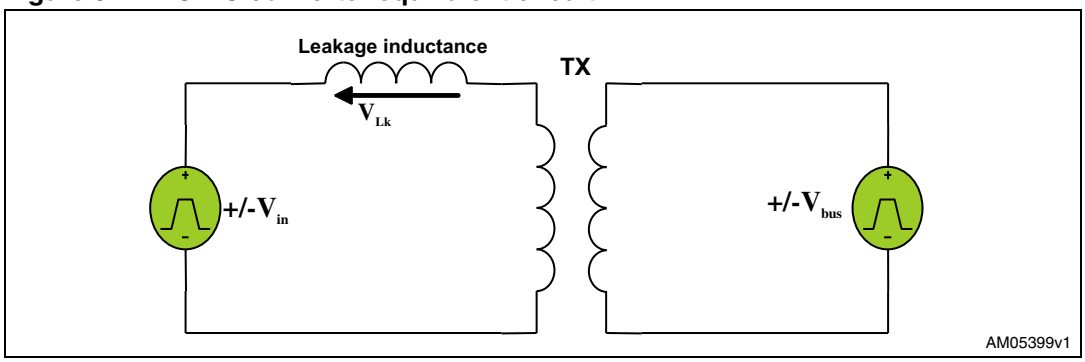
Figure 4. DC-DC converter control signals



The same drive signal used for device M1 also controls M4, as the one controlling M3 is also used for M2. The effect of the input bridge modulation is to generate a square wave on the

input of the HF transformer which varies between +Vin and -Vin, while the effect of the modulation on the active rectifier is to generate, on the secondary of the HF transformer, a square wave varying between +Vbus and -Vbus, where Vbus is the voltage on capacitor C2, phase shifted with respect to the primary one of an angle δ, equal to the phase shift of the modulating signals, as shown in the equivalent circuit of figures *5*, *6*, *7*, *8*, *9*, *10*, and *11*.

Figure 5. DC-DC converter equivalent circuit



As a result, the primary voltage and the secondary transformer voltage reflected to the primary determine the rising and falling slope of the current in the leakage inductance. According to leakage inductance current waveforms, two operating modes may be distinguished for the converter:

- Discontinuous current mode DCM
- Continuous current mode CCM

Both in CCM and DCM, three main operating modes or intervals may be distinguished in half the switching period. Considering the modulation shown in *Figure 9*, in CCM the leakage inductance current may be calculated as follows:

- Mode 1, interval (t_0 - t_1):

At t_0 M1 and M4 are turned on at ZVS, M6 is also on. The voltage across the leakage inductance is:

Equation 1

$$V_{LK} = V_{in} + \frac{V_{bus}}{n}$$

and the current may be written as follows:

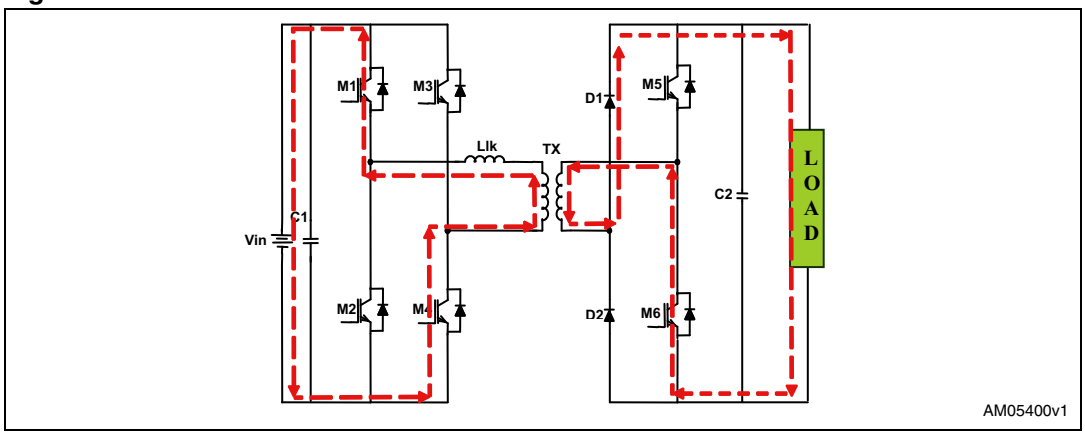
Equation 2

$$i_{Lk}(t) = \frac{1}{L_k} V_{in}(1+d)(t-t_1) + i_{Lk}(t_0)$$

$$d = \frac{V_{bus}}{V_{in} \cdot n}$$

Since this current is negative, as shown in *Figure 9*, it flows in the circuit as demonstrated in *Figure 6*.

Figure 6. Current flow in mode 1



This mode ends when leakage inductor current reaches zero at $t=t_1$.

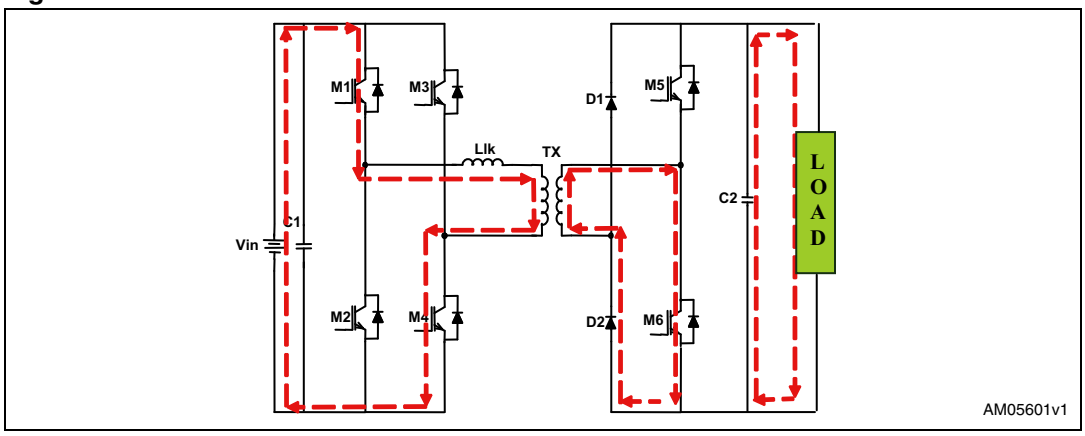
- Mode 2, interval (t_1-t_2):

When the leakage inductor current reaches zero, D1 and D2 turn-off with soft switching, as the current naturally reaches zero. After $t=t_1$ M6 is still on, primary current changes polarity and flows through M1 and M4. On the secondary side the transformer is shorted through M6 and D2, as shown in *Figure 7*. Inductor current may be written as:

Equation 3

$$i_{Lk}(t) = \frac{1}{L_k} V_{in}(t - t_1) + i_{Lk}(t_0)$$

Figure 7. Current flow in mode 2



- Mode 3, interval (t_2-t_3):

At $t=t_2$ M6 is turned off and M5 is turned on under ZVS. A positive voltage equal to +Vbus is applied on transformer secondary winding. Leakage inductor current is given by:

Equation 4

$$i_{LK}(t) = \frac{1}{L_k} V_{in}(1-d)(t - t2) + i_{Llk}(t_2)$$

The current path in the circuit is drawn in *Figure 8*.

Figure 8. Current path in mode 3

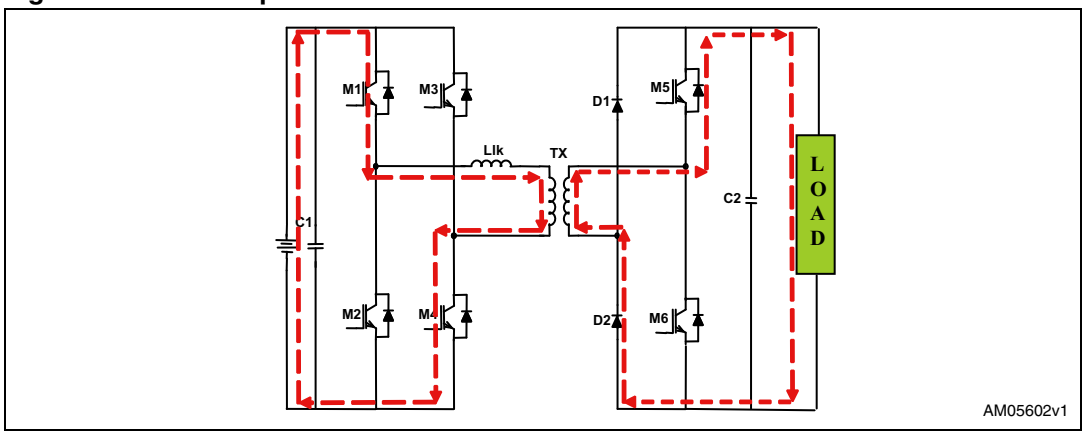
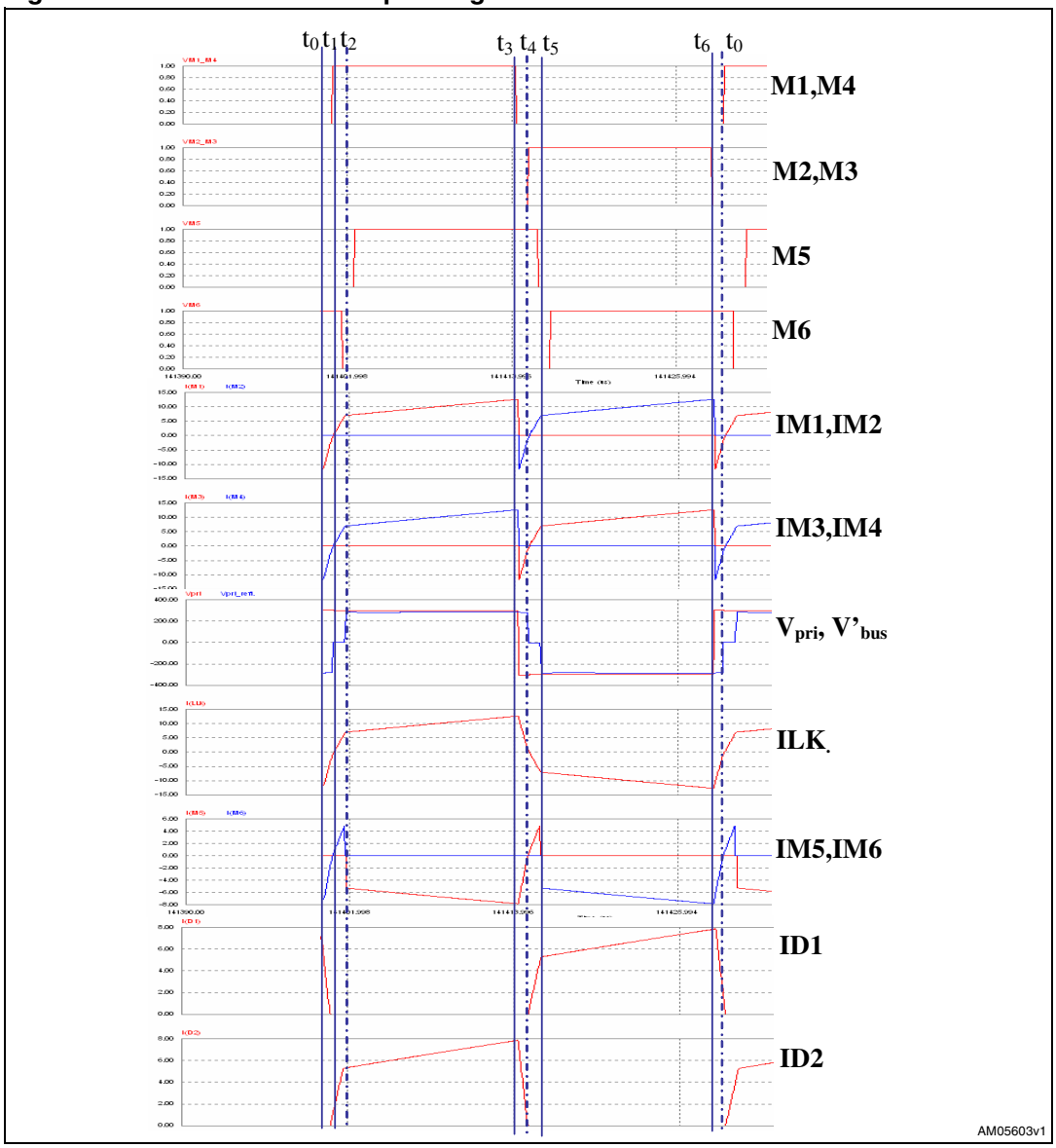


Figure 9. DC-DC converter operating waveforms



Due to symmetry during the two halves of the switching period, current expressions and current paths may be derived with similar considerations for the second half of the switching period.

If d >1 the current in the leakage inductor may reach zero and there is a boundary between CCM and DCM.

In DCM there are also three modes of operation, as shown in *Figure 10*.

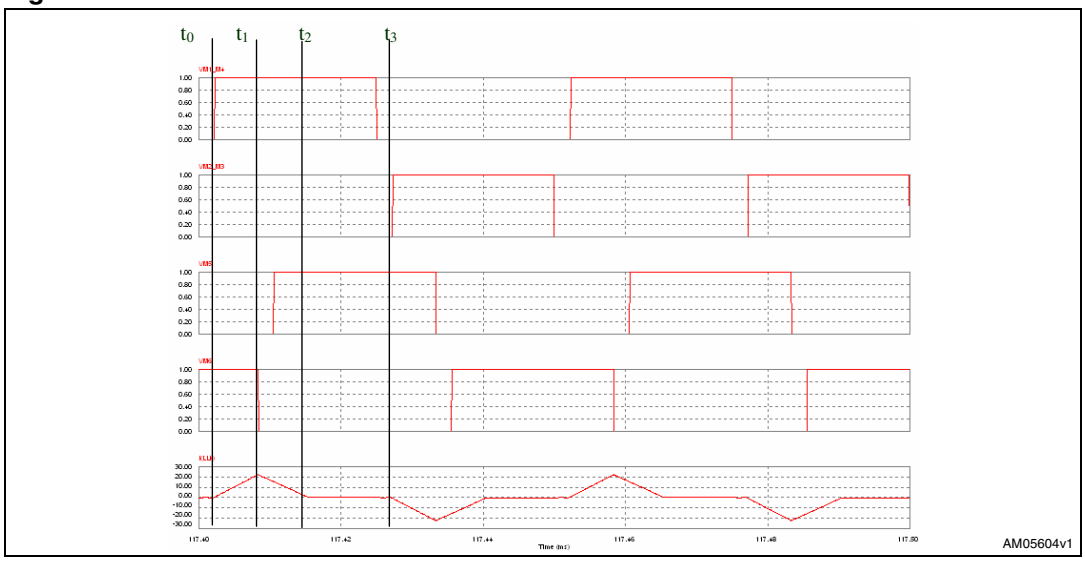
- Mode 1, interval t_0-t_1:

At $t=t_0$ inductor current is zero. After $t=t_0$ devices M1and M4 are turned on under zero current and inductor current rises according to the following equation:

Equation 5

$$i_{Lk}(t) = \frac{1}{L_k} V_{in}(t - t_1) + i_{Lk}(t\ )$$

Figure 10. Modulation and transformer current in DCM



- Mode 2, interval t_1-t_2:

At t_1 M6 turns off and M5 turns on with zero current. Inductor current expression is given by:

Equation 6

$$i_{LK}(t) = \frac{1}{L_k} V_{in}(1-d)(t - t_2) + i_{Llk}(t_2)$$

and reaches zero at $t=t_3$.

- Mode 3, t_2-t_3

Equation 7

$$i_{LK}(t) = 0$$

The boundary between DCM and CCM depends on the phase-shift angle, input voltage, output voltage and transformer turns ratio and is given by:

Equation 8

$$\phi_B = \frac{d-1}{d}\pi$$

By integrating the leakage current expression over the switching period and multiplying the result by the input voltage value the expression of power transfer may be derived as:

Equation 9

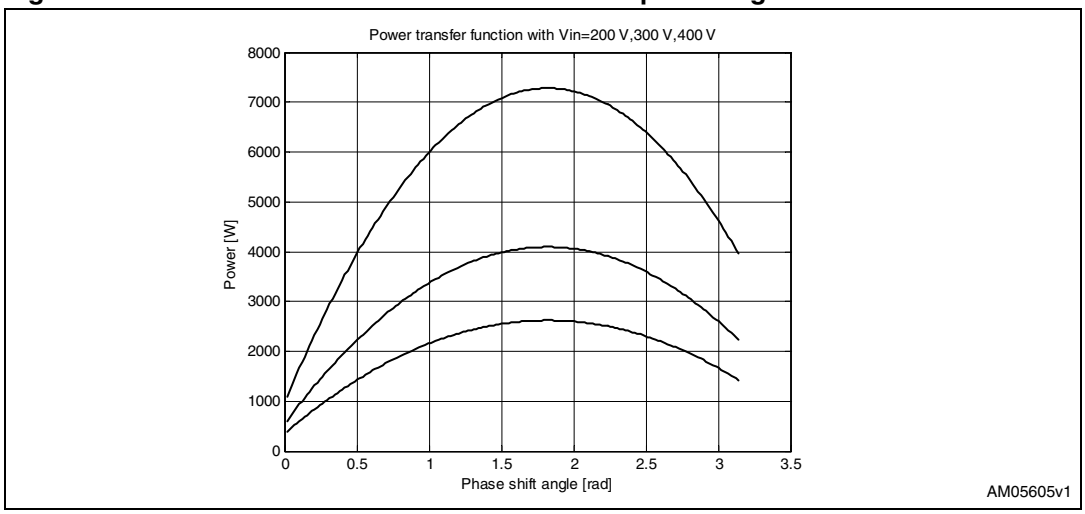
$$\begin{cases} P = \frac{V_{in}^2}{\omega_s L_k}\frac{d}{2\pi(d-1)}\phi^2 & \phi < \phi_B \\ P = \frac{V_{in}^2}{\omega_s L_k}\frac{d}{2(2+d)^2}\cdot F(\phi) & \phi > \phi_B \end{cases}$$

where $\omega_s=2\pi f_s$ is the switching frequency in rad/s, $\phi=\omega_s t$ is the phase-shift angle and

$$F(\phi) = \pi(1+d-2d^2) + 4\phi(1+d+d^2) - 2\frac{\phi^2}{\pi}(2+2d+d^2)\cdot$$

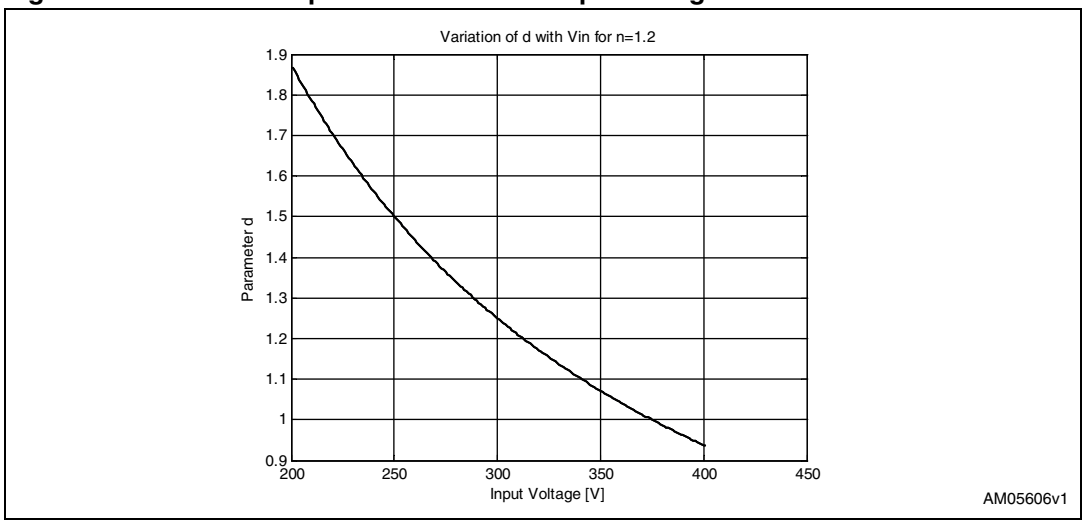
once the operation of the converter has been described, based on the specification in *Table 1*, the power transfer function may be plotted as shown in *Figure 11*.

Figure 11. Power transfer function for different input voltages



As the converter operates in boost mode the value of parameter “d” must be kept greater than “1” for every value of input voltage in order to maintain controllability, also at low power levels. In fact, if d<1 the converter is characterized by a minimum power level under which the converter cannot be controlled. For this reason, transformer turns ratio has been chosen at equal to 1.2. The value of leakage inductance must also be chosen carefully and it is a compromise between peak current value and the maximum energy transfer between input and output.

Figure 12. Variation of parameter “d” with input voltage for n=1.2



A leakage inductance value comprised between 35 µH and 55 µH is suitable to obtain the desired power level of 3 kW in all the input voltage range for the chosen transformer turns ratio of 1.2.

3 DC-DC converter design

After having described the operation of the DC-DC converter, the design may be completed according to the specifications in *Table 1*.

- Input power: assuming 90 % efficiency the input power is:

Equation 10

$$P_{in} = \frac{P_{out}}{0.9} = 3333\ W$$

- Maximum average input current:

Equation 11

$$I_{in} = \frac{P_{in}}{V_{inmin}} = \frac{3333}{200} = 16.66\ A$$

- Maximum average output current:

Equation 12

$$I_{out} = \frac{P_{out}}{V_{outmin}} = 7.5\ A$$

- Maximum input power device RMS current value:

Equation 13

$$I_{rms} = 2\sqrt{D_{max}}I_{in}\sqrt{\frac{1+K+K^2}{3(K+1)^2}}$$

Where K=0 for triangular waveforms and K=1 for rectangular waveforms. This said, the maximum RMS current value in DCM is:

Equation 14

$$I_{rms\_DCM} = 2\sqrt{D_{max}}I_{in}\sqrt{\frac{1+K+K^2}{3(K+1)^2}} = 2\sqrt{\frac{D_{max}}{3}}I_{In} = 13.6\ A$$

And assuming K=0.6 for trapezoidal current waveform in CCM:

Equation 15

$$I_{rms\_CCM} = 2\sqrt{D_{max}}I_{in}\sqrt{\frac{1+K+K^2}{3(K+1)^2}} = 2\sqrt{D_{max}}I_{In}1.15 = 27.2\ A$$

- Minimum input power device breakdown voltage:

Equation 16

$$V_{Brk_{Mos}} = 1.3 \bullet V_{MPPTmax} = 1.3 * 400 = 520\ V$$

- Transformer turns ratio:

As the converter operates in boost mode, to avoid problems of controllability for low power levels, the value of parameter “d” must always be greater than one:

Equation 17

$$d \geq 1 \rightarrow n \leq \frac{Vout}{dVin_{MAX}} \leq 1.12$$

Moreover, considering the voltage drop across the leakage inductor it is possible to operate the converter with n=1.2 without incurring regulation problems for high input voltage values at low power.

- Minimum output power device breakdown voltage:

Equation 18

$$V_{Brk_{Mos}\_OUTPUT} = 1.2 \bullet V_{MPPT_{max}} * n = 1.2 * 400 = 576\ V$$

- Power device selection:

According to the calculations above, four STW55NM60ND MOSFETs were selected for the input bridge and also two STW55NM60NDs for the active rectifier. The main characteristics of this MOSFET are reported in *Table 2* and *3*:

Table 2. MOSFET electrical characteristics

VDS@Tjmax	RDSon_max	ID@100°C	Coss	Qg
650 V	0.06 Ω	29 A	900 pF	190 nC

- Rectifier diode selection:

Two STTH60L06s are selected for the diode leg. The main characteristics are shown in *Figure 3*:

Table 3. Diode rectifier electrical characteristics

Vf_max @150 °C IF=60 A	Vrrm	Trr_max	IF	IRM
1.4 V	600 V	85 n	60 A	10.5 A

- Input capacitor value:

The input capacitor, C1, is designed to smooth the high frequency ripple at the input of the PV array. If the current generated by the module is assumed to be constant and the current drawn by the converter is assumed to be a pulse train, the following equation gives the value of the input capacitance:

Equation 19

$$C_1 > \frac{P_{array}}{2f_s \Delta v_{array} Vin_{min}}$$

where:

P_{array} is the PV field maximum output power, ΔV_{array} is the allowable peak-to-peak voltage ripple at the input of the array, f_s is the switching frequency and Vin_{min} is the minimum operating value for the input voltage. Assuming 90 % efficiency for the converter and 0.1 % of admissible peak-to-peak ripple voltage the input capacitance value is:

Equation 20

$$C_1 > \frac{P_{array}}{2f_s \Delta v_{array} Vin_{min}} = \frac{3333.33}{2 * 35000 * 0.2 * 200} = 1.1\,mF$$

Three 330 µF, 450 V electrolytic capacitors are connected in parallel at the input of the converter to limit the effect of the high frequency ripple on the PV generator.

- Output capacitor value:

In a similar way the value of the C2 bus capacitor may be calculated, taking the fact that the ripple is sinusoidal at twice the grid frequency into account:

Equation 21

$$C_2 > \frac{P_{out}}{2\omega_{grid} \Delta v_{bus} V_{bus}} = \frac{3000}{2 * 2 * \pi * 50 * 9 * 450} = 1.17\ mF$$

where the peak-to-peak voltage of 9 V corresponds to a voltage ripple of 1 % of the nominal bus voltage and the grid frequency is 50 Hz.

- HF transformer design:

The design is based on the core geometry method. The transformer specifications are shown in *Table 4*:

Table 4. HF transformer specifications

Specification	Symbol	Value
Nominal input voltage	V_{in}	300 V
Maximum input voltage	V_{inmax}	400 V
Minimum input voltage	V_{inmin}	200 V
Input current	I_{in}	27 A
Nominal output voltage	V_{out}	450 V
Output current	I_{out}	22.5 A
Switching frequency	f	35 kHz
Efficiency	η	99 %
Regulation	α	0.15
Max operating flux density	B_m	0.15 T
Window utilization	K_u	0.3
Duty cycle	D_{max}	0.5
Maximum temperature rise	T_r	70 °C

The transformer apparent power is:

Equation 22

$$P_t = \frac{P_0}{\eta} + P_0 = (\frac{1}{\eta} + 1)V_0 I_0 = 6061\,W$$

Then the electrical condition parameter calculation K_e may be evaluated:

Equation 23

$$K_e = 0.145 \bullet K_f^2 \bullet f^2 \bullet B_m^2 \left(10^{-4}\right)$$

where Kf=4.44 is the waveform coefficient.

Equation 24

$$K_e = 0.145(4.44)^2(35.000)^2(0.15)^2\left(10^{-4}\right) = 7606$$

Now, the core geometry parameter is calculated as:

Equation 25

$$K_g = \frac{P_t}{2K_e\alpha} = 2.65\ cm^5$$

The Kg parameter of a generic transformer core is given by the following equation:

Equation 26

$$K_{g_{CORE}} = \frac{W_a A_c^2 K_u}{MLT}$$

Using two sets of E70/33/32s the following condition is verified:

Equation 27

$$K_{g_{CORE}} = \frac{W_a A_c^2 K_u}{MLT} > K_g$$

The number of primary turns for the design flux swing is:

Equation 28

$$N_1 = \frac{V_{in_{min}} D_{max} T}{\Delta B \cdot 2 \cdot A_c} = 14 turns$$

The primary inductance value is:

Equation 29

$$L_p = N^2 A_L = (14)^2 * 12666\ nH = 2.48\ mH$$

and the number of secondary turns is:

Equation 30

$$N_2 = n \bullet N1 = 17 turns$$

The next step is to choose the wire size in order to realize primary and secondary windings. At 35 kHz, current penetration depth is:

Equation 31

$$\delta = \frac{6.62}{\sqrt{f}} = 0.035 \text{ cm}$$

Then, the wire diameter may be selected as follows:

Equation 32

$$d = 2\delta = 0.07 \text{ cm}$$

And the conductor section is:

Equation 33

$$A_W = \pi\frac{d^2}{4} = 0.0038 \text{ cm}^2$$

AWG21, having d=0.072 cm and a wire area of $A_{W_{AWG22}}$=0.0040 cm^2, may be used for this design. Considering a current density of J=500 A/cm^2, the number of primary wires is given by:

Equation 34

$$S_{np} = \frac{A_{wp}}{A_{w_{AWG26}}} = 13.5 \rightarrow \text{choose} \quad S_{np} = 14$$

where

Equation 35

$$A_{wp} = \frac{I_{rmsCCM}}{J} = 0.054 \text{ cm}^2$$

Since the AWG21 has a resistance of 420 µΩ/cm, the primary resistance is:

Equation 36

$$r_p = \frac{420 \text{ } \mu\Omega/\text{cm}}{14} = 30 \text{ } \mu\Omega/\text{cm}$$

and so the value of resistance for the primary winding is:

Equation 37

$$R_p = N_1 \cdot 2 \cdot MLT \cdot r_p = 13.7 \text{ m}\Omega$$

With the same procedure for the secondary winding it is:

Equation 38

$$A_{ws} = \frac{I_{rms\_CCM}}{n \cdot J} = 0.045 \text{ cm}^2 \quad S_{ns} = \frac{A_{ws}}{A_{wawg21}} = 11 \quad r_s = \frac{420 \text{ } \mu\Omega/\text{cm}}{11} = 38 \text{ } \mu\Omega/\text{cm}$$

$$R_s = N_2 \cdot 2 \cdot MLT \cdot r_s = 21.1 \text{ m}\Omega$$

The total copper losses are:

Equation 39

$$P_{Cu} = P_p + P_s = R_p I^2_{in} + R_s I_s^2 = 20.9\ W$$

From the core loss curve of N87 material, at 100 °C, 0.15 T and 35 kHz, the selected core has the following losses:

Equation 40

$$P_V = 20\frac{kW}{m^3} \bullet 2 \cdot V_e = 4\ W$$

Where V_e=102000 mm^3 is the core volume of one set of E75/33/32.

The efficiency of the transformer is:

Equation 41

$$\eta_T = \left(1 - \frac{24.9}{3000}\right) * 100 = 99.17\%$$

The transformer temperature rise is:

Equation 42

$$T_r = 0.5 \cdot R_{th} \bullet (P_{Cu} + P_V) = 79.68\ ^oC$$

With

Equation 43

$$R_{th} = 6.4\ \frac{^oC}{W}$$

4 DC-AC converter

The DC-AC inverter is a standard single-phase full bridge based on IGBTs with ultrafast co-pack diodes, as depicted in *Figure 3*. The connection to the grid is realized by means of current control performed in DQ rotating reference frame. An LCL filter is placed between the bridge and the grid in order to reduce the current harmonics generated by the unipolar sinusoidal pulse-width modulation (USPWM) at 17 kHz. L filters or LC filters may also be chosen for the application, but in the first case large values of inductance are required to perform good high frequency noise damping and large currents through the capacitor may arise in the second case together with high voltage harmonics. LCL filters show good performance in terms of current harmonic reduction but they may lead to instability of the control loop in the presence of large grid impedance. This instability is due to the presence of extra poles introduced by the additional inductor. The problem may be solved with proper filter design and by adding a damping resistor in series with the filter capacitor.

The value of L_f is designed in order to limit the current ripple to about 10 % of the nominal current value according to:

Equation 44

$$L_f = \frac{\left(V_{BUS} - V_{grid\_pk}\right)\cdot D}{2\cdot \Delta i \cdot f_{sw}} = \frac{(450-324)*0.72}{2*1.3*17000} = 2.05\ \text{mH}$$

The filter capacitor value is designed to limit the exchange of reactive power below 5 % of nominal active power:

Equation 45

$$P_{reactive} = \frac{V_{grid}^2}{X_c} \le 0.05P_n$$

$$X_c \ge \frac{V_{grid}^2}{0.05P_n} = 352.6\ \Omega$$

$$C \le \frac{1}{\omega X_c} = 9\ \text{uF}$$

To avoid resonance problems for the filter, due to low and high order harmonics, its resonant frequency, given by $f_{res} = \frac{1}{2\pi}\sqrt{\frac{L_g + L_f}{L_f L_g C_f}}$, should be in a range between ten times the line

frequency and one half of the switching frequency:

Equation 46

$$10 * f_{grid} \le f_{res} \le 0.5 f_{sw}$$

$$500\ \text{Hz} \le f_{res} \le 8.5\ \text{kHz}$$

In fact, if the resonant frequency is too small the filter resonance increases the low frequency harmonics and, in the same way, if it is too high it increases the harmonics multiple of the switching frequency.

With a filter capacitor value of 3.3 µF and a grid inductor value of 2 mH the resulting resonant frequency is 2771 Hz, which is in the specified range.

The LCL filter is effective only if proper damping is added. Passive damping, realized with a resistor series connected to the filter capacitor was used for this application. The value of the resistor is chosen to be one third of the impedance of the capacitor at the resonant frequency:

Equation 47

$$R_{damp} = \frac{1}{3 * \omega_{res} * C} = 5.8\ \Omega$$

- Selection of semiconductor devices

The semiconductors selected for the DC-AC section are 600 V, 35 A IGBTs with internal fast diodes used to minimize the effect of recovery at turn-on. The choice of IGBTs is a trade off between cost and efficiency. The part number of the device used is STGW35HF60WD, which shows very good performance in terms of switching losses. The electrical characteristics of this device are shown in *Table 5*.

Table 5. STGW35HF60WD electrical characteristics

Part number	Saturation voltage	Collector current	E_{off}	E_{on}	Gate charge
STGW35HF60WD	VCE_{sat} @125 °C,13 A	I_C@100 °C	E_{off} @125 °C,15 A	E_{on} @125 °C,15 A	Q_g
	1.8 V	37 A	360 µJ Rg=47 Ω	300 µJ Rg=56 Ω	102 nC

The power losses in each IGBT may be calculated considering conduction losses, switching losses and diode losses.

Conduction and switching losses in IGBTs may be evaluated according to the following equations:

Equation 48

$$Pcond = V_{CE} * I_{pk}\left(\frac{1}{2\pi} + \frac{1}{8} ma \cos\phi\right) + R_{CE} * I^2_{pk} * \left(\frac{1}{8} + \frac{ma}{3\pi}\cos\phi\right) = 9.6\ W$$

$$Psw\_on = \frac{Eon}{\pi} f_{sw} = 1.94\ W$$

$$Psw\_off = \frac{Eoff}{\pi} f_{sw} = 1.62\ W$$

Where

$$V_{CE} = 1.8\ V$$

$$ma = \frac{V_{grid\_pk}}{V_{bus}} = \frac{325}{450} = 0.72$$

$$\cos\phi = 1$$

$$R_{CE} = 0.02\ \Omega$$

Diode losses may be evaluated according to the following equations:

Equation 49

$$P_{diode\_DC} = V_F * I_{pk} * (\frac{1}{8} - \frac{ma}{3\pi}\cos\phi) = 1.3\ W$$

$$P_{diode\_RR} = \frac{1}{8} I_{rr} t_{rr} V_{pk} f_{SW} = 0.45\ W$$

where

Equation 50

$$V_{pk} = 450\ V \qquad I_{rr} = 5.4\ A \qquad t_{rr} = 88\ ns$$

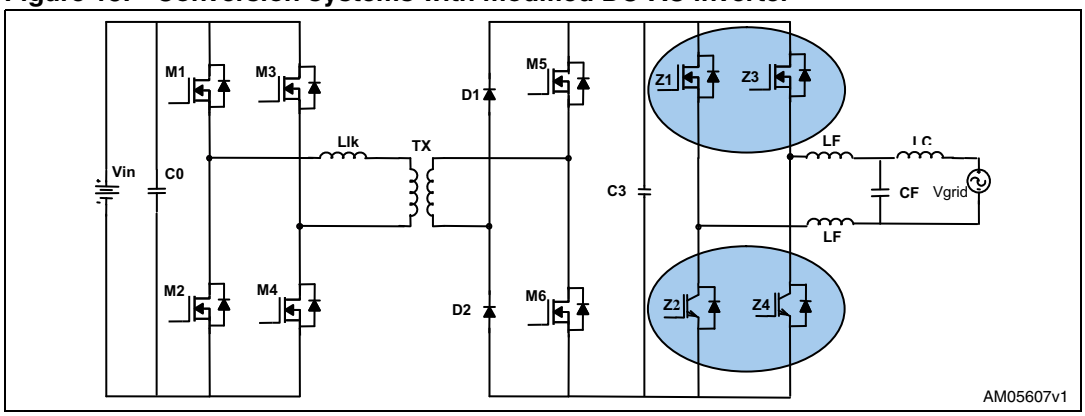
The resulting total losses for the single-phase inverter are calculated below:

Equation 51

$$P_{tot} = 4(P_{diode\_DC} + P_{diode\_RR} + Psw\_on + Psw\_off + Pcond) = 59.6\ W$$

resulting in 98% theoretical efficiency for the inverter stage. A simple modification of the control strategy, together with a different choice of power devices, may improve the efficiency and performance of the DC-AC stage. The modified circuit is shown in *Figure 13*.

Figure 13. Conversion systems with modified DC-AC inverter



The low-side power devices, Z2 and Z4, are low-drop IGBTs switching at 50 Hz according to grid polarity while the high-side devices are MOSFETs switching at high frequency with pulse-width modulation. Compared to the standard topology, the main advantages are lower conduction losses of both MOSFETs and low-drop IGBTs, absence of switching losses for the low-side devices and, eventually, the possibility of using higher switching frequencies with a reduction of reactive components size and cost and wider bandwidth for the control loop.

The possible implementation of this solution may be based on the use of STW55NM60ND for the high-side and STGW35NB60SD, connected in parallel to an external SiC diode, for the low side. A gain in efficiency between of 0.5 % and 1 % may be measured with such an implementation.

5 Schematic description

The power board schematic is shown in *Figure 14*. The input voltage, produced by the PV array and comprising between 200 V and 400 V, is fed to the power circuit through connector J7. The input filter consists of 3 high voltage electrolytic capacitors and two 0.1 µF polypropylene capacitors connected at the input of the bridge, to reduce the effects of parasitic inductances due to cables and PCB tracks. Each of the four input power MOSFETs, STW55NM60ND, are connected in parallel to a STTH30R06, 600 V 30 A ultra-fast, soft recovery diode. This diode carries only a small amount of current during ZVS operation of the DC-DC converter due to the relatively lower forward voltage of the MOSFET body diode.

The power MOSFETs in the active rectifier are connected in parallel to 4.7 nF, 630VDC polypropylene capacitors used as voltage snubbers to minimize turn-off losses.

The HF transformer is realized using two E70/33/32 cores with N87 ferrite. In a transformer having only a primary and a secondary winding, the value of the leakage inductance is determined by the number of turns in each of the two windings and by the spatial arrangements of these windings. The leakage inductance increases with an increasing number of turns and with an increasing distance between the windings. However, the spatial arrangement of the windings cannot be chosen arbitrarily, mainly because of mechanical restrictions introduced by the core geometry chosen for the specific application. Then, if a high value of leakage inductance is needed, an additional coil may be added in series to the primary or a bigger core may be selected for the transformer. The leakage inductance of the transformer in this application is designed without an additional external coil to achieve a more compact set-up and lower cost.

A bank of four 330 µF, 500 V electrolytic capacitors, connected in parallel, is placed on the inverter bus to filter the 100 Hz ripple, together with a 2.2 µF, polypropylene capacitor to

filter the high frequency component generated by the DC-DC converter. The output of the DC-DC converter is connected to J9, a two-way connector mounted on the PCB in

order to allow the independent operation of both conversion stages. For example, by connecting an electrical load to J9 and a DC voltage source to J7 the operation of the DC-DC converter may be evaluated independently from the inverter. In the same way, connecting a DC voltage source to J9 and disabling the modulation of the DC-DC converter the operation of the DC-AC inverter may be evaluated both in standalone or grid-connected operation. In standalone mode of operation the system is controlled in open loop, while in grid connection mode the system operates with closed loop control.

The full bridge inverter consists of two legs implemented with STGW35HF60WD IGBTs.

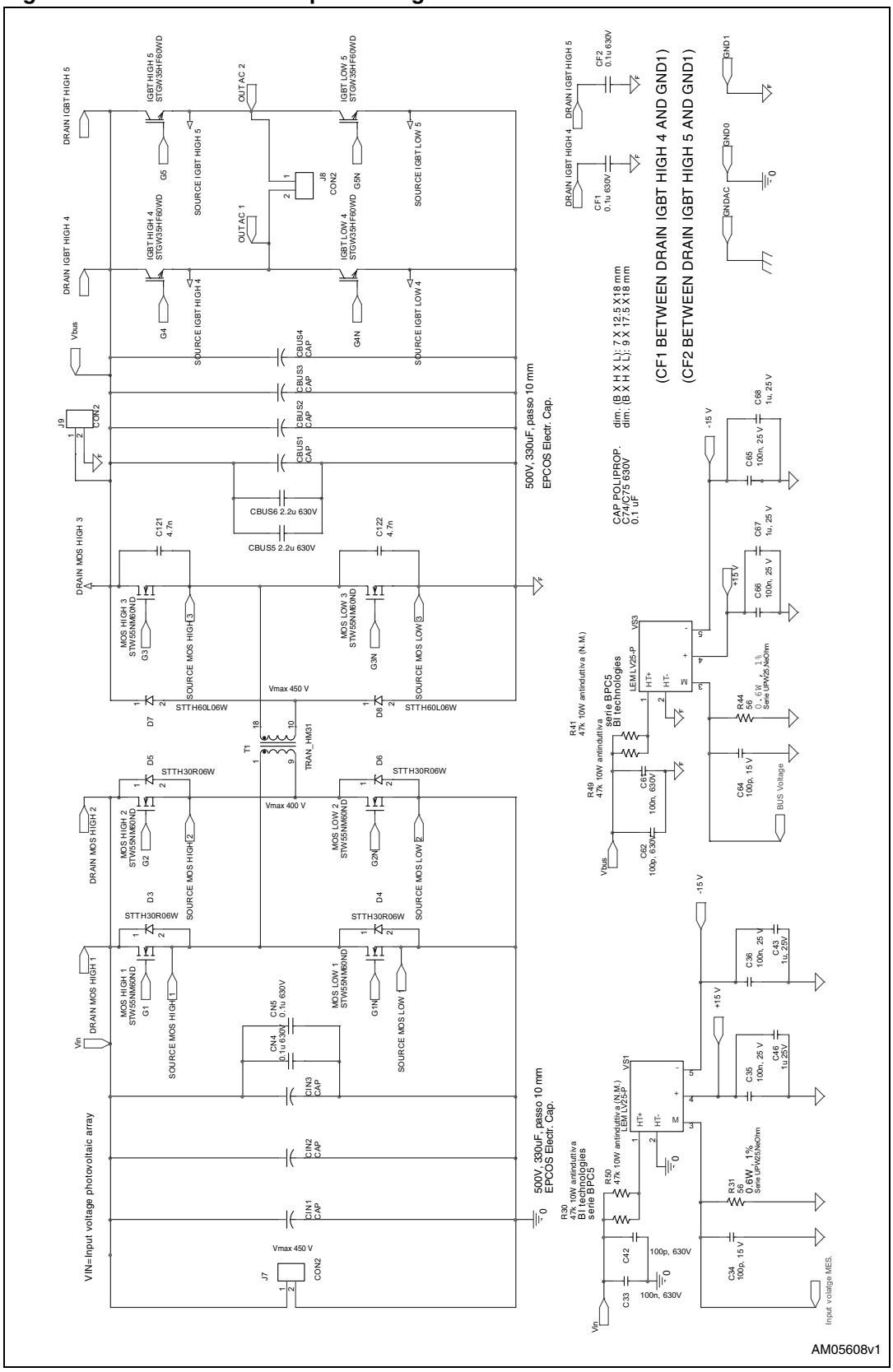
A 0.1 µF, 630VDC polypropylene capacitor (CF1, CF2) is connected across each leg. The mid point of each leg is then reported on J8 to allow the connection of the two 1 mH inductors used as high frequency filters together with capacitor C1 (*Figure 15*). This capacitor, placed on the output sensing and relays board, is connected to the filter inductors through a two-way connector J7, placed on the same board. The current in the filter inductor is sensed by means of a Hall effect sensor CS1 and is used as a feedback for the control algorithm. Also the grid voltage, sensed with LV1, is a feedback for the control algorithm and is used for current synchronization to obtain unitary power factor.

Hall sensors provide inherent galvanic isolation between the grid and the control circuitry and are very simple to use, requiring only a +15 V/-15 V supply voltage and a measurement resistor. Despite these advantages, their cost is higher compared to other sensing solutions.

For example, a cheaper solution may be implemented using a simple voltage divider or a shunt resistor together with an analog opto-isolator to provide galvanic isolation between the power stage and control section. The price to pay in this case is the added complexity of the sensing circuitry.

The physical connection to the grid is realized by means of two relays, placed on line and neutral, which are controlled by an I/O of the control board with the STM32F103xx microcontroller, and supplied by the 24 V bus generated by the multi-output power supply. The feedback signals are sent to the control board by means of coaxial shielded cables connected to J14 and J15 on the relays board.

Figure 14. Schematic of the power stage



The output voltage of the sensor circuits must be adapted to the voltage range of the analog to digital converter (ADC) of the STM32F103xx microcontroller, which is 0-3.3 V. This task is accomplished using simple circuits based on operational amplifiers, such as the one shown in *Figure 16* for grid-voltage measurement.

Figure 15. Output sensing and relay board schematic

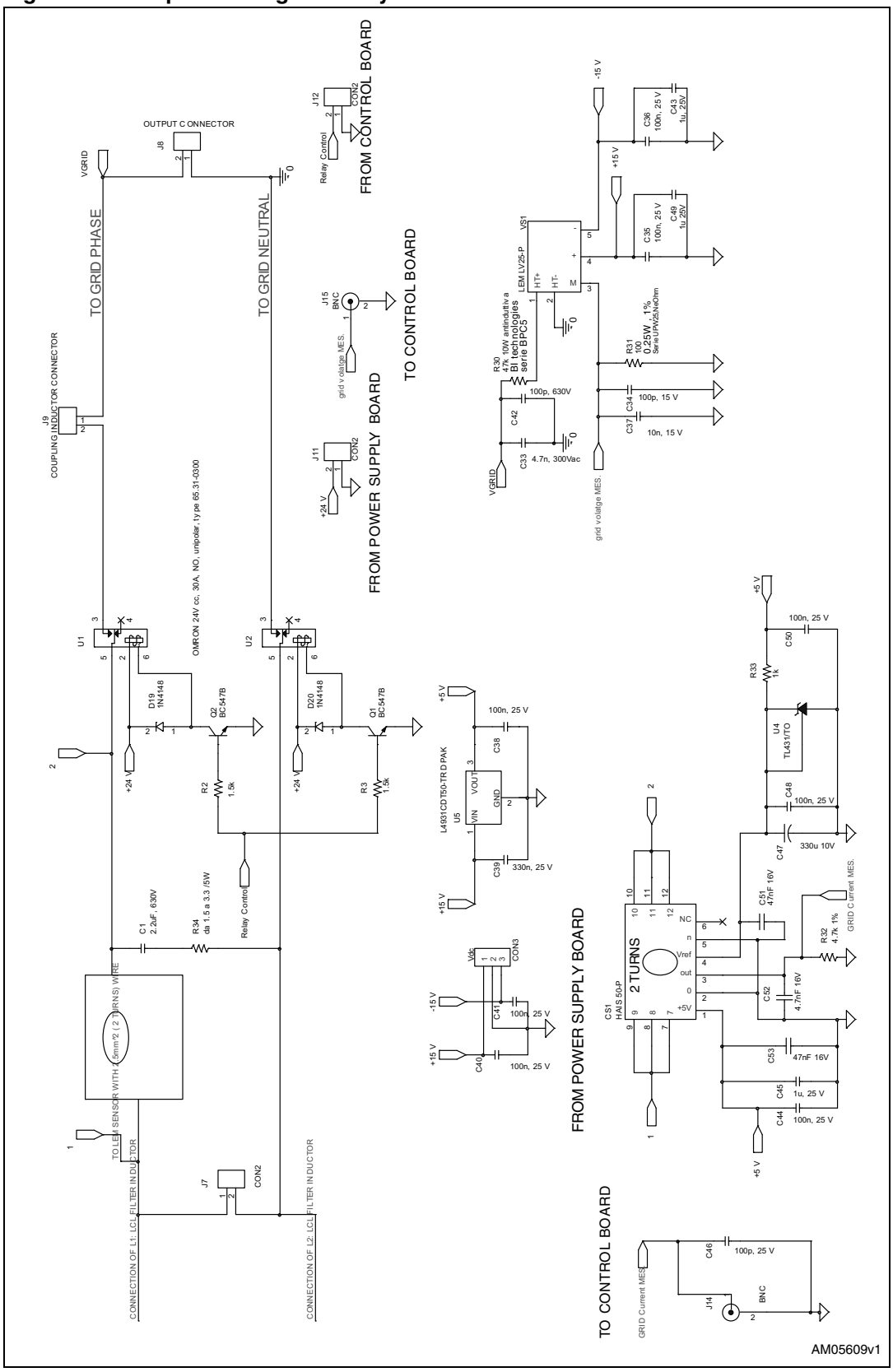
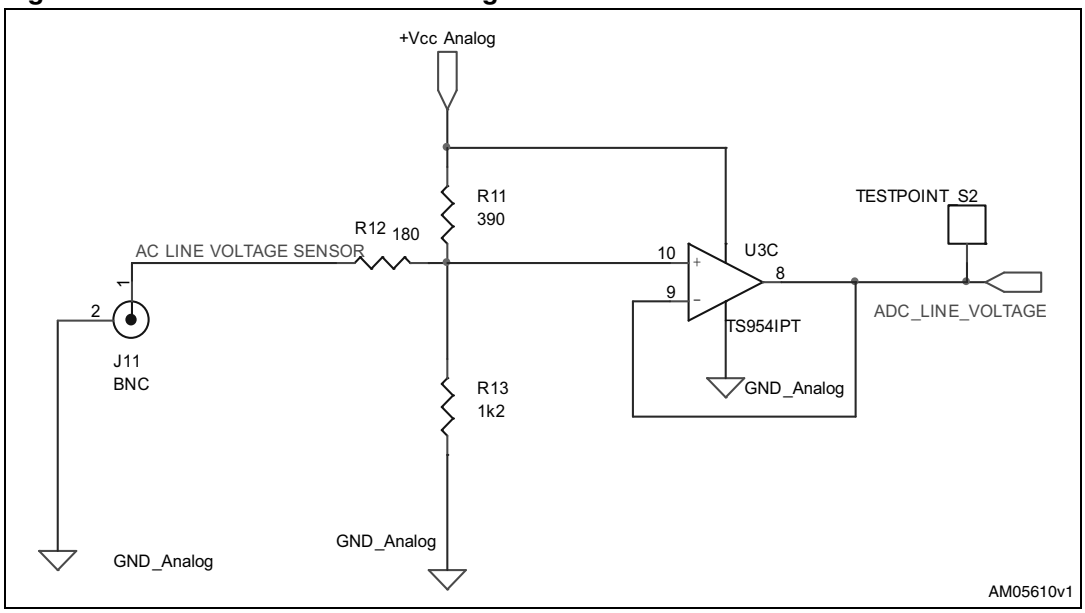


Figure 16. Schematic of the AC voltage measurement circuit



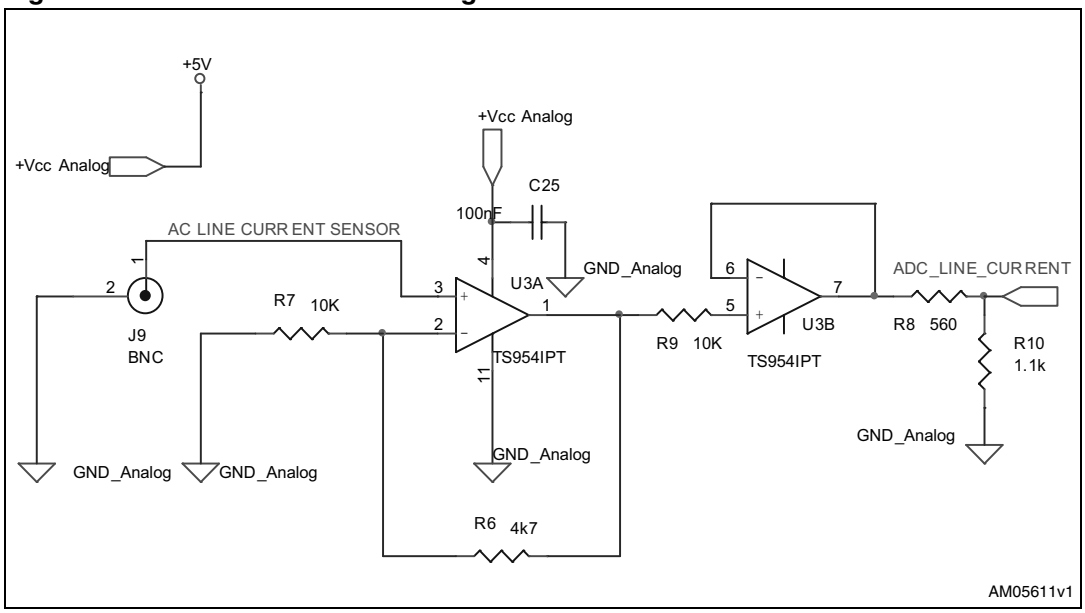
The circuit is supplied by the 5 V bus generated by the multi-output power supply and the measured voltage is fed through connector J11. The output voltage of this circuit is then equal to the sum of the measured voltage plus an offset voltage according to the following equation:

Equation 52

$$V_{out} = V_{meas.}\frac{R11//R13}{R12+R11//R13} + V_{cc}\frac{R13//R12}{R11+R13/R12}$$

Where V_{meas} is the voltage on J11, V_{cc} is the 5 V supply voltage and V_{out} is the voltage on pin 8 of the operational amplifier. The line current conditioning circuit was designed in a similar way and the electrical scheme is shown in *Figure 17*:

Figure 17. Line current conditioning circuit



In this case the output voltage is given by:

Equation 53

$$V_{out} = \frac{R10}{R10 + R8} \cdot V_{meas.} \left(1 + \frac{R6}{R7}\right)$$

Where: V_{meas} is now the voltage output of the current sensor, having an offset of 2.5 V generated by a TL431 configured as the voltage reference.

The same circuit in *Figure 17* is used for the sensing of the DC bus voltage, PV array voltage and PV array current.

In summary, the overall control architecture requires five feedback signals for correct operation, input current and input voltage are used for maximum power point tracking; inverter bus DC voltage, grid voltage and grid side current are used for grid-tied operation and current injection. These signals are sent to the ADC inputs of the microcontroller, according to the pin assignment of *Figure 19* and sampled at 17.4 kHz (*Figure 18*).

Figure 18. ADC interrupt service routine

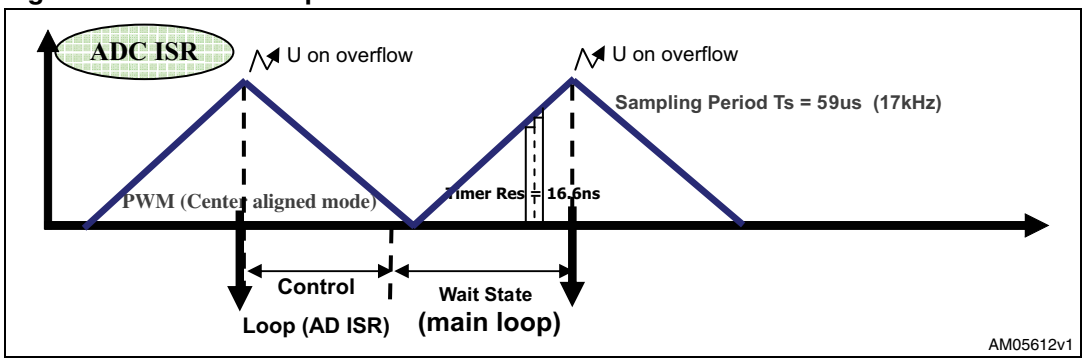


Figure 19. STM32F103xx microcontroller schematic

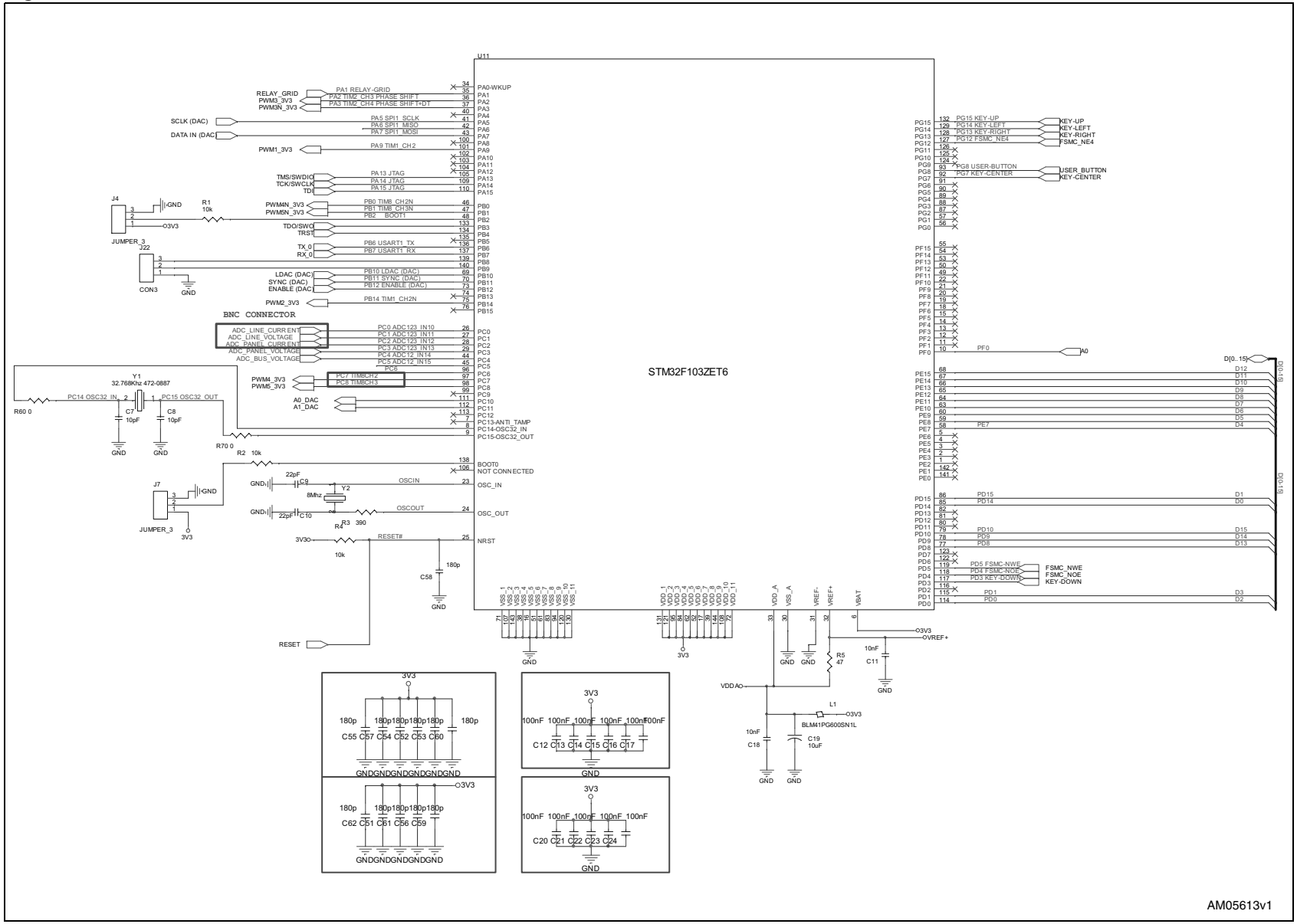


Figure 20. DC-DC converter driver

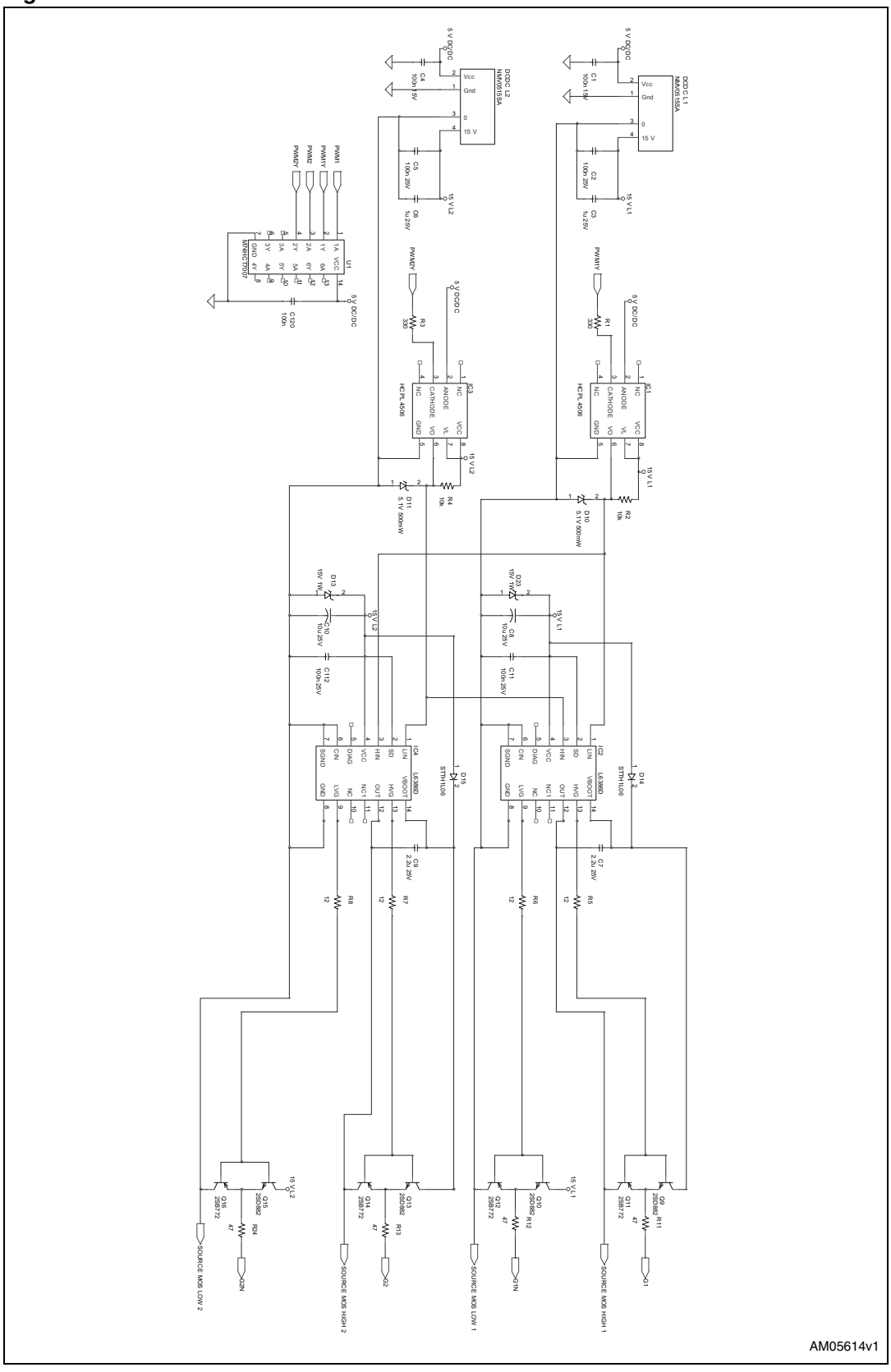
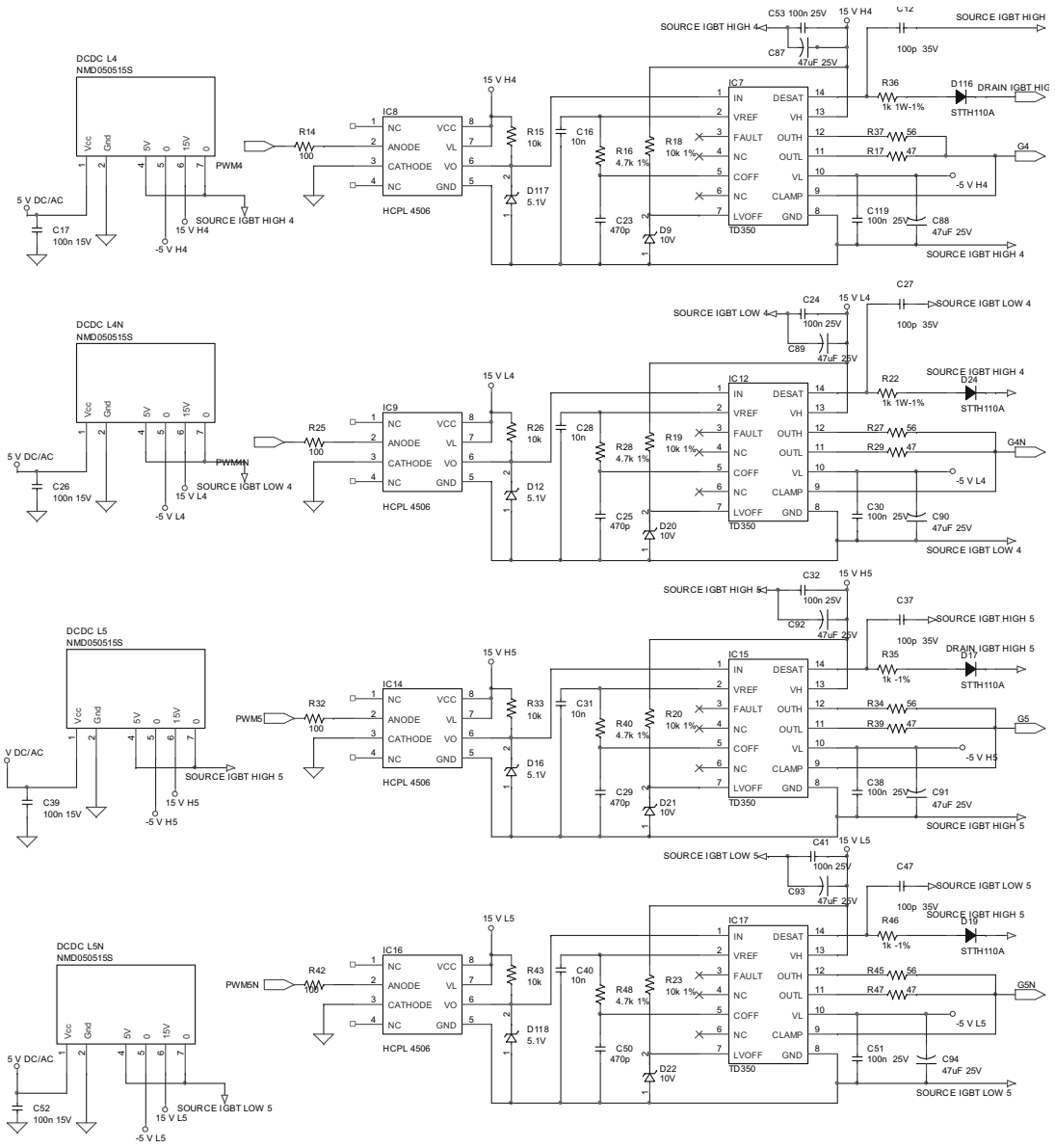


Figure 21. DC-AC converter driver



The outputs of the microcontroller are the PWM signals used to control the power devices in each leg of the conversion system.

Power MOSFETs and IGBTs must be interfaced to the control circuit while maintaining galvanic isolation. Two slightly different solutions were implemented for the DC-DC and the DC-AC converter. In the first, a L6386 IC with a bootstrap capacitor for a floating drive supply was selected because of the low cost and the capability of driving a high-side and a low-side device with a single IC, therefore simplifying the layout of the board. The opto-isolator receives the signal generated by the microcontroller and performs the level shifting of this signal from 0-5 V to 0-15 V. The opto-isolator output pin is connected to the L6386 input pin. A totem pole circuit, consisting of a PNP-NPN BJT pair, connects the output of the IC to the gate of each MOSFET, amplifying the driving current and allowing fast switching, both at turn-on and turn-off. The +15 V supply voltage of the IC and opto-isolator is provided by an isolated DC-DC converter, as shown in *Figure 20*. A similar solution was used to drive the IGBTs in the inverter bridge. The main difference is the use of a single driver IC, TD350, characterized by 0.75 A/1.2 A source/sink current capability and includes some dedicated control and protection functions such as IGBT desaturation, two level turn-off and fault detection output. The circuit implemented is shown in *Figure 21*.

Figure 22. 5 V,1 A flyback converter with VIPER17HN

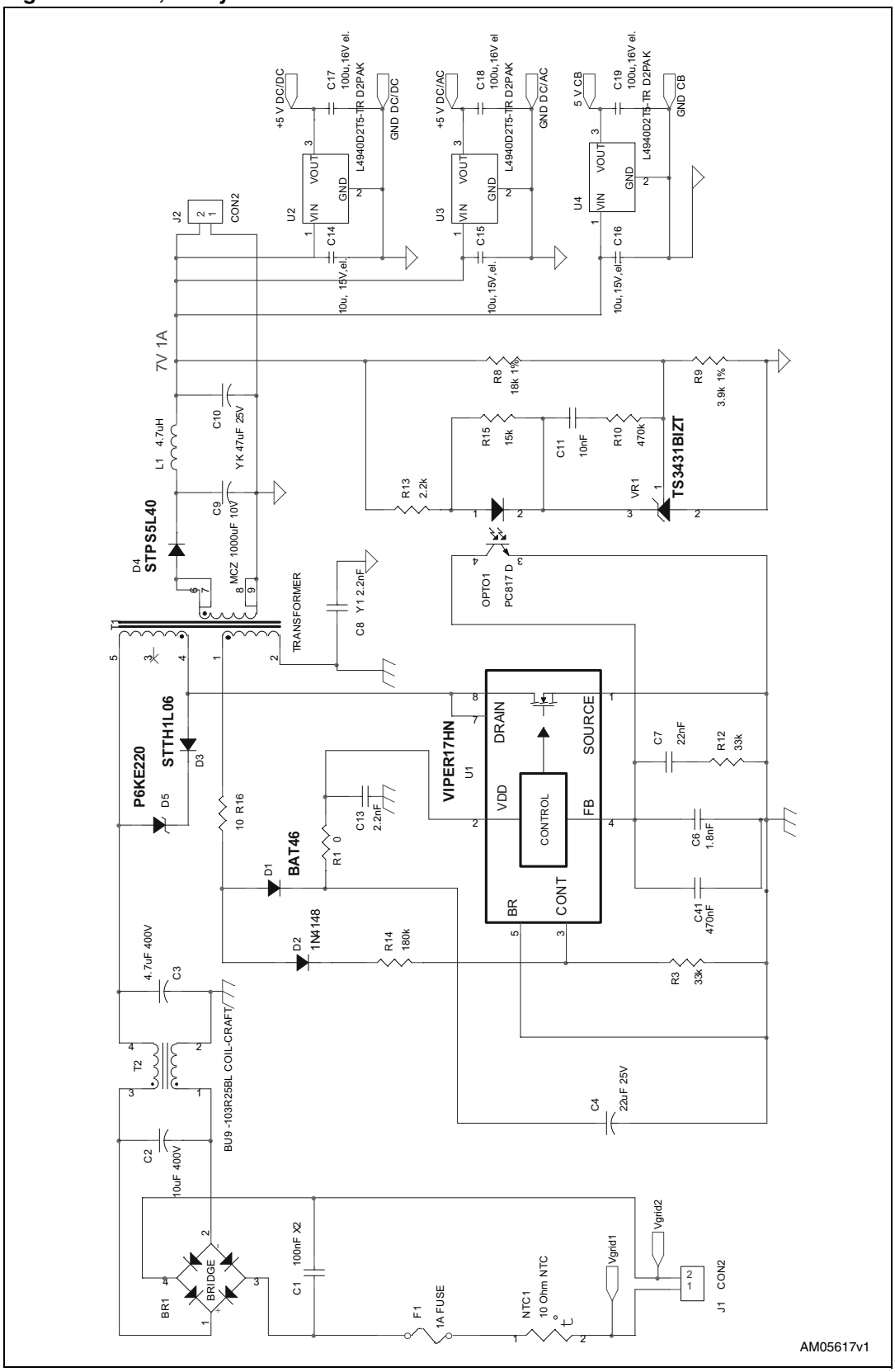
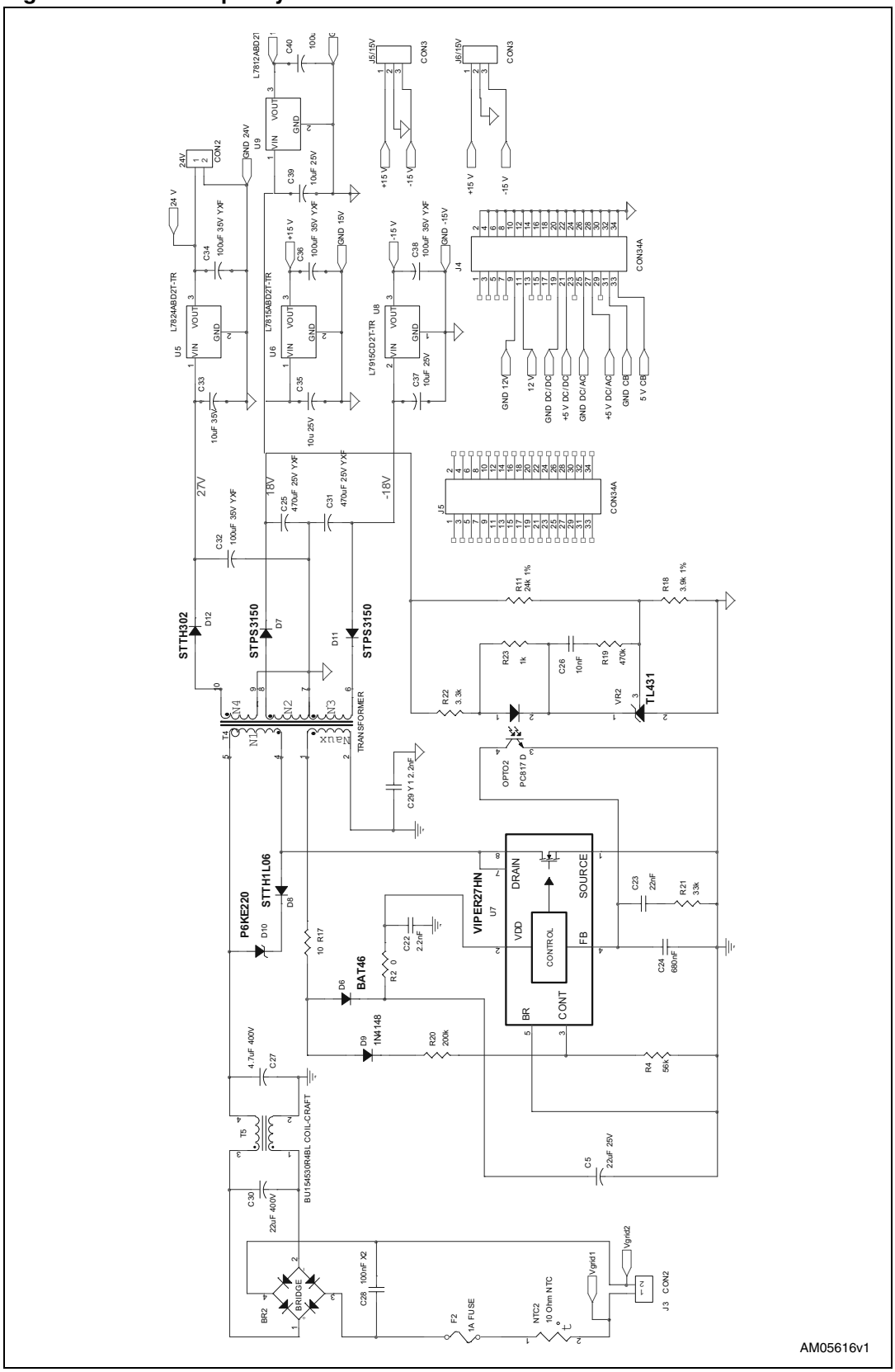


Figure 23. Multi-output flyback converter with VIPER27HN



The isolated DC-DC converters used in the driver circuits are supplied by a 5 V bus generated by an offline flyback converter, with wide input voltage, using VIPER 17HN according to the electrical scheme of *Figure 22*. The circuit is capable of delivering up to 5 W and feeds the control circuitry of the main DC-DC converter, the DC-AC inverter and the control board through 5 V voltage regulators.

In a similar way, the 24 V and +/-15 V bus is generated with a VIPER27HN device, implementing a multi-output flyback solution.

6 STM32F103xx-based current control strategy for inverter grid connection

A single-phase grid-connected inverter, with unipolar pulse-width modulation, operates from a DC voltage source and is characterized by four modes of operation or states. Two modes take place during the positive load current period and two modes in the negative load current period, as shown in *Table 6*.

Table 6. Operating modes of grid-connected voltage source inverter

Mode	Z1	Z2	Z3	Z4	D3	D4	V_{out}	I_{out}
1	On	Off	Off	On	Off	Off	Vbus	+
2	On	Off	Off	Off	On	Off	0	+
3	Off	On	On	Off	Off	Off	-Vbus	-
4	Off	On	Off	Off	Off	On	0	-

The switching patterns are defined by a control algorithm which generates the desired outputs starting from the information provided by the feedback signals. For example, algorithms for the grid connection are based on the use of current controllers, consisting of a single loop or multiple loops according to the desired level of dynamics and accuracy. Multiple-loop controllers are generally preferred, thanks both to their superior performance and the relative ease of implementation in modern microcontrollers. With single-voltage loop control methods, the inverter output voltage is compared with a sinusoidal reference, proportional to the grid voltage and the generated error is then sent to the input of a current regulator to create a sinusoidal reference for the PWM modulator. Despite its simple implementation, this approach does not provide good regulation under non-linear loads and is characterized by steady-state error. For these reasons, both output voltage and current are used in control algorithms to provide better dynamic response and damping of the resonant peak caused by the output LC or LCL filter. However, the time varying nature of the controlled variables prevents an optimal regulation of output voltage and current. To overcome such problems, a predictive current controller or deadbeat controller may be implemented. The first approach, based on the assumption that a precise model of the controlled system is available, predicts the inverter voltages required to force the measured current to follow the reference current, but has the disadvantage of being difficult to implement. The second method, while providing really fast dynamic response, is very sensitive to system noise and is dependent on system parameters, [see *References 12*, *13*, *14*, *15*, *16*].

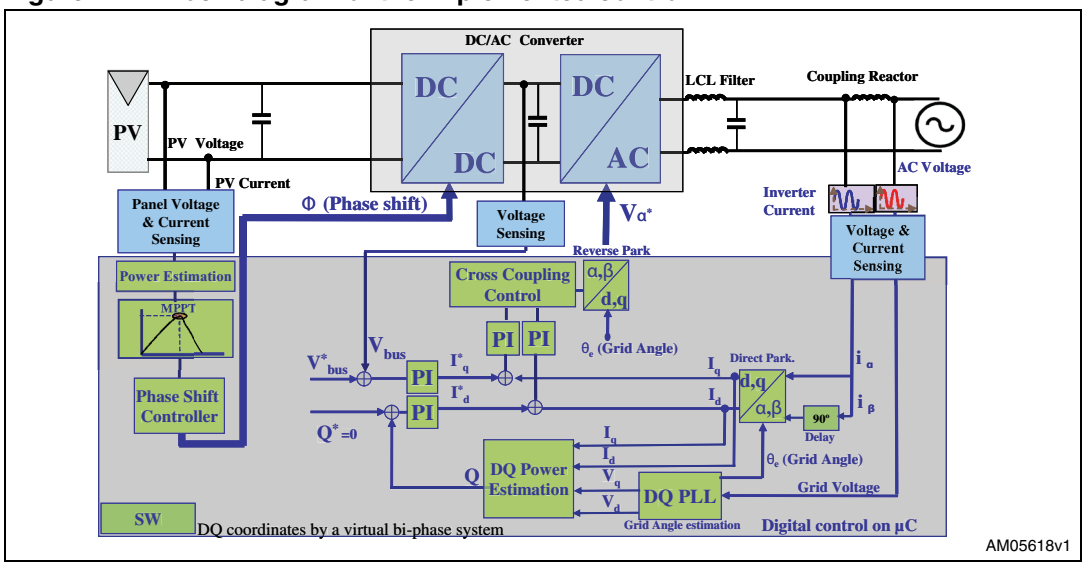
Recently, new methods such as the PR (proportional resonant) current control method have been adopted to control the PV inverters with zero steady-state error and the possibility of selective harmonic compensation with low computational effort. However, implementations in low cost fixed-point microcontrollers have been proven to be difficult due to limited computational capability and restricted numerical representation.

Another possible current-control method uses DQ synchronous reference frames and provides both the advantage of zero steady-state error, thanks to the use of PI controllers, and simple implementation.

For these reasons, this method was implemented on a 32-bit ARM-based STM32F103xx microcontroller and its performance was verified through simulations and experimental results on the grid connected inverter.

A block diagram of the implemented control algorithm is shown in *Figure 24*.

Figure 24. Block diagram of the implemented control



Every algorithm for grid-connected inverter operation is based on the estimation or direct measurement of grid-voltage frequency and phase angle. Both parameters are fundamental for correct operation and special care must be taken in their detection to avoid the influence of any external noise. The detection method used in this implementation for a single-phase inverter is based on a synchronous reference frame PLL. While in three-phase inverters the use of DQ based PLL is quite common, for single-phase inverters, the necessity of a virtual bi-phase system arises. In fact, to create a rotating DQ reference, starting from a stationary frame, at least two independent phases are required. This problem is overcome with the creation of a virtual voltage, V_β, phase-shifted with respect to the real grid voltage, V_α, of 90°. This task may be easily accomplished with firmware. If the two voltage components V_α and V_β are available, the transformation from the stationary reference frame to the DQ rotating frame is given by:

Equation 54

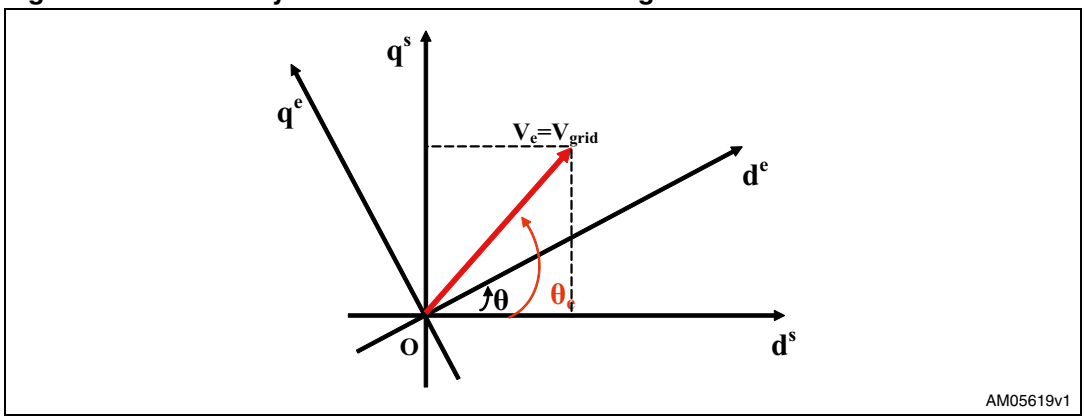
$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \cdot \begin{bmatrix} V_\beta \\ V_\alpha \end{bmatrix}$$

where θ is the angle between the DQ reference frame and the stationary reference frame (*Figure 25*). The reverse transformation is given by:

Equation 55

$$\begin{bmatrix} V_\beta \\ V_\alpha \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \cdot \begin{bmatrix} V_d \\ V_q \end{bmatrix}$$

Figure 25. Stationary reference frame and rotating reference frame



Where

Equation 56

$$\begin{bmatrix} V_\beta \\ V_\alpha \end{bmatrix} = \begin{bmatrix} V_m \cos\theta_e \\ V_m \sin\theta_e \end{bmatrix}$$

Then the two components on the DQ reference frame are:

Equation 57

$$Vd = V_m \cos\theta_e \cos\theta + V_m sen\theta_e sen\theta = V_m \cos(\theta - \theta_e)$$
$$Vq = -V_m \cos\theta_e \sin\theta + V_m \sin\theta_e \cos\theta = V_m \sin(\theta - \theta_e)$$

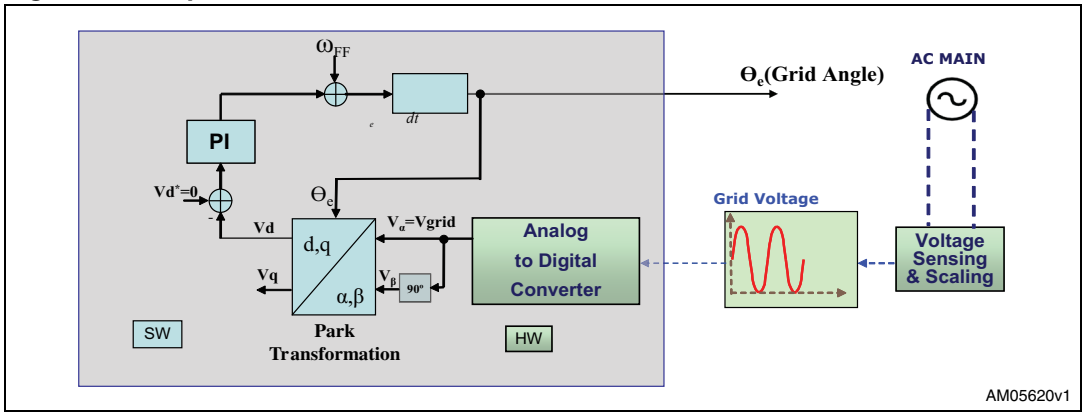
Therefore, if $\theta=\theta_e$ the two components are reduced:

Equation 58

$$Vd = V_m$$
$$Vq = 0$$

In order to detect the grid-voltage angle, used to perform the transformation, a PLL structure may be used. In *Figure 25*, the block diagram of the PLL implemented in this application is shown.

Figure 26. Implemented PLL structure



The grid voltage and the 90° phase-shifted voltage are used to perform the reference frame change, or “park transformation”, and create two voltage components on the DQ reference frame called V_d and V_q. One of the two components is controlled to zero with a PI regulator. The output of the PI regulator is the grid frequency which may be integrated to obtain the grid angle.

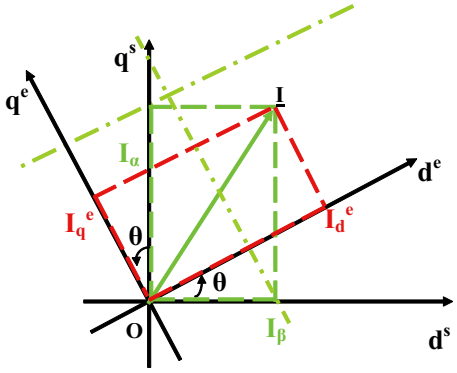
It is worth knowing that if the V_q component is controlled to zero then the V_d component follows the grid-voltage rotation. In this case, the active power injected into the grid may be controlled, transforming the current in the same reference frame and by acting on the amplitude of the Id component. The Iq component must also be controlled in order to ensure zero reactive power injection. On the contrary, if the V_q component is controlled to zero in the PLL, the active power is controlled with the Iq current component and the Id current component is used to control the reactive power to zero or to the desired value.

This said, the advantages of such a control structure are clear: first of all the current components on the synchronous reference frame are constants and may then be controlled with standard PI regulators ensuring zero steady-state error; the second advantage is a decoupled control of active and reactive power.

The reference values for the active and reactive component of the current are set by two additional PI regulators in the outer control loop. The active reference current component is generated by confronting the DC bus voltage with the reference voltage value. The error between the actual value and the reference DC bus voltage is sent to a PI regulator whose output is the active current component value (*Figure 26*).

Similarly, the reactive current reference value is set by another PI regulator whose input is the error generated between the reactive power command and the actual estimated value.

Figure 27. DQ components of the current

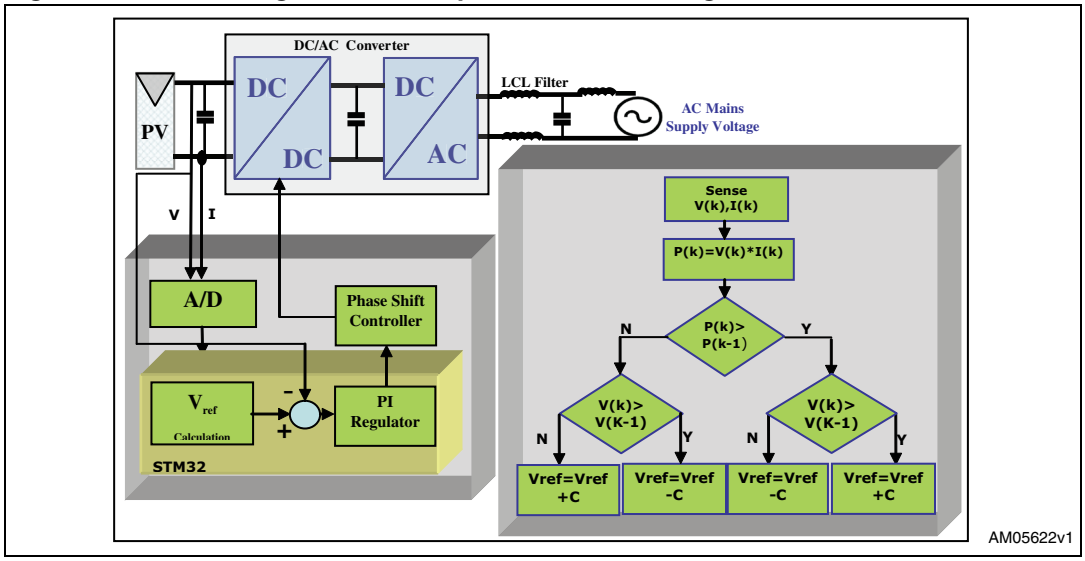


The difference between reference components of the current and the actual DQ components are the inputs of the PI regulators in the inner control loop. The outputs of the PI regulators in the inner loop are two voltage components, V_d and V_q. By performing a reverse park transformation, two AC voltages are generated back to the stationary reference frame, and therefore the generation of the modulating signals of the DC-AC converter may be executed by the microcontroller.

The amount of power injected into the grid depends on the power available from the PV array. This power is then processed by the DC-DC converter which is controlled in order to maximize the energy yield from the array, independent to temperature variations and irradiation conditions, by controlling its input impedance. The control of the input impedance requires both PV array current and voltage sensing and some simple calculations executed

by the well known maximum power point algorithm. The main functions of the MPPT algorithm are shown in *Figure 28*.

Figure 28. Block diagram of the implemented MPPT algorithm



The block diagram is an explanation of the perturb and observe (P and O) method, a very common and easy way to implement an MPPT technique. The PV array voltage is compared to a constant reference voltage, which corresponds, once the algorithm has reached the convergence, to the PV array voltage at the maximum power point, under specific atmospheric and temperature conditions. The error signal is used as the input of a PI regulator which generates a command (phase-shift angle) used to drive the power devices of the DC-DC converter. The reference voltage is the output of the flow chart of *Figure 27* where, based on the calculation of PV output power by sampling input voltage and current values, the power change is detected, by comparing the present and previous voltage levels, together with the change of the input voltage. Therefore, the reference voltage is incremented or decremented according to both array power and voltage change, [see *References 17*, *18*].

Apart from gird connection and MPPT, some other functions are implemented for the correct operation of the conversion system. The following is a brief description of these functions:

- Input voltage control

Input voltage value is constantly monitored to ensure that the array voltage is always in the correct operating range, between 200 V and 400 V. The voltage value is also utilized to minimize the conversion ratio between the input and output of the DC-DC converter. For example, if the input voltage is between 200 V and 250 V the output voltage is regulated at 400 V. For higher input voltage values the reference bus DC voltage is regulated at 450 V. In this way, the conversion ratio for the DC-DC converter is minimized and the efficiency improved. If the input voltage value is below 200 V or above 400 V, the input under/overvoltage protection is enabled. Consequently, the modulation is disabled in both stages and the relays disconnect the system from the grid. For the sake of security the complementary pairs must be disabled synchronously in case of power stage failure/fault and this is performed by a dedicated emergency stop input embedded in the peripheral.

- Input current control

The same kind of strategy is used to detect any condition of overcurrent in the system. This protection is enabled when the average input current is above 18 A.

- Bus DC voltage control

The output of the bus DC is controlled in order to stabilize the inverter input voltage to the bus DC reference voltage. The minimum DC bus voltage is a function of the peak-to-peak AC line voltage in order to minimize total harmonic distortion (THD) of the injected current. This limit depends on grid-voltage fluctuations and may be calculated according to the following equation:

Equation 59

$$V_{busref\_min} = \sqrt{2}\left(V_{grid\_max} + \frac{P_{dc} * Z_c}{V_{grid\_max}}\right)$$

where P_{dc} is the average power on the DC bus, V_{grid_max} is the maximum RMS value of the grid voltage and Z_c is the output LCL filter impedance. In other words, the DC bus must never decrease below the peak grid-voltage value plus the drop across the IGBTs and the LCL filter. To ensure safe operation, this voltage must never surpass the protection threshold of 480 V.

In case of bus DC under/overvoltage the system is disconnected from the grid according to the strategy already described.

- Burst mode operation at startup

In the case of an overcurrent or overvoltage event, the DC-DC converter modulation is first disabled by the control algorithm. Then, the DC-DC modulation is disabled and the interface relays are disconnected, preventing any power flow from the system to the grid. After that, the control algorithm performs some checks on the input voltage, bus DC voltage, grid-voltage and grid-frequency value. If the sensed voltages are in the allowable range (200-400 V input, 380-450 V bus DC, 230 Vrms +/- 10 %, 49.7 Hz-50.3 Hz grid voltage) the DC-DC converter is started in burst mode in order to charge the bus DC voltage at the reference voltage level. This same check procedure is executed at startup, before the connection to the grid is actually performed. During burst mode of operation the DC bus voltage is regulated with hysteretic control. The boundary values of the hysteresis window Vb_1, Vb_2 are chosen to limit the DC bus voltage ripple to 5 % of the reference value. Once the bus capacitor is charged, the control loop mode of operation is enabled and the connection to the grid performed.

- Line voltage and frequency detection and anti-islanding

The PLL continuously measures the line voltage and frequency in all operating states. If the voltage or frequency exceeds the high or low limits, the inverter ceases to deliver power to the grid. These conditions are also used to implement a passive method for island operation detection. An island operation occurs when the utility power is disconnected for maintenance or fault reasons while the inverter is still delivering power. With a passive method, detection of islanding from the utility grid is achieved via AC under/overvoltage and under/overfrequency detection functions.

- Output overcurrent

Due to fault conditions or AC line transient conditions, the maximum current may be exceeded. In this case, the inverter ceases to deliver power to the grid according to the strategy explained above. The current threshold value is set to 15 A.

- Open loop operation

This mode of operation was implemented to allow system debug independently from grid operation. This mode, used for maintenance, test and debug, allows system operation only with manual control by acting on a set of pushbuttons on the microcontroller board. The DC-DC converter power transfer may be adjusted by acting on the phase-shift parameter through the pushbutton placed on the microcontroller board. In the same way, the power transfer of the DC-AC converter may be modified acting on the modulating index.

The dead time of the power bridges in each converter may also be adjusted.

- LCD display

The microcontroller board is equipped with a graphic LCD display. The selectable functions are:

1. Open-loop mode
2. Closed-loop mode
3. Calibration
4. DC-DC converter manual control
5. DC-AC converter manual control

It is important to note that the calibration function must be performed by the operator when the system is first connected to the grid. In this way, any offset affecting the feedback signals used for control mode operation is compensated via firmware. When the calibration function is executed the display shows a grid current offset of about 2.5 V and a grid-voltage offset of about 1.8 V.

7 Experimental results

Control issues have been thoroughly investigated and the possibility of implementing the algorithm using a 32-bit ARM-based microcontroller from STMicroelectronics is verified. The dedicated control board, developed for this purpose, is equipped with an STM32F103xx microcontroller, characterized by a 32-bit CORTEX TM-M3 core with suitable peripherals. The core, running at 72 MHz, is able to perform up to 90 MIPS. A high performance CPU, based on Harvard architecture, plus suitable peripherals such as two advanced PWMs, fast and accurate 12-bit A/D conversions with double S and H circuit and high resolution timers, allows the implementation of very sophisticated control algorithms.

The control loop has been synchronized with the A-D conversions triggered by the ON states of the two PWM timers. This brings benefits in terms of accuracy, avoiding the acquisition of analog quantities (e.g. currents) during commutations of the power devices. The execution time of the most relevant tasks is reported in *Table 7*.

Table 7. Execution time of the main control functions

Function	Execution time
n.5 A/D acquisitions	1 µs
MPPT	1.5 µs
DQ_PLL+internal PID	10 µs
Direct park transf	5 µs
PI regulator	3 µs each
Reverse park transf	5 µs
Sine modulation	1.5 µs
Total control loop execution time @ 72 MHz	≅ 30 µs

The entire control loop is executed in about 30 µs (50 % CPU-load) with a sampling time of 57 µs. Further code may be executed in the remaining 50 %, allowing the implementation of a HMI (human machine interface) such as LCD driving or a graphical user interface via SPI, in order to have a complete smart-platform.

For this application, the three main control issues regarding a PV converter, namely, MPPT, grid synchronization and power management control, have been included within the firmware. All the PWM signals, necessary for power management, are generated with proper dead-time, settable with a resolution of 16.6 ns by acting on the firmware developed for this application. The algorithm may control both the active and reactive power in the DQ synchronous frame, while the implemented MPPT algorithm is based on the P and O method and may be optimized with simple modifications to the source code. The inverter current is transformed, using Park equations, in the two components referred to the rotating DQ reference frame of the grid voltage. These components, Id and Iq, are proportional to active and reactive generated power, respectively. The reference current value of q axis, I*q, is calculated in order to regulate the voltage of the DC bus Vbus. Reactive power is maintained at zero through I*d, as only the injection of active power into the mains is allowed, according to international standards. PI outputs are transformed back into AC quantities, using the inverse park transformation, providing the signals for inverter modulation. The most critical task of the power management control is the estimation of the

grid angle. The required software and hardware operations of the PLL have been performed with the same microcontroller used for the main digital control. The experimental results may be seen in *Figure 29* and *30*, where the grid angle (in yellow) is drawn together with the voltage component on the d axis (green track) of the synchronous reference frame, which is controlled to zero. *Figure 31* shows the synchronization between the estimated angle and the two voltages on the stationary reference frame, namely, the grid voltage (red track) and the 90° phase-shifted voltage (blue track), [see *References 19*, *20*].

Figure 29. Grid angle and V_d component

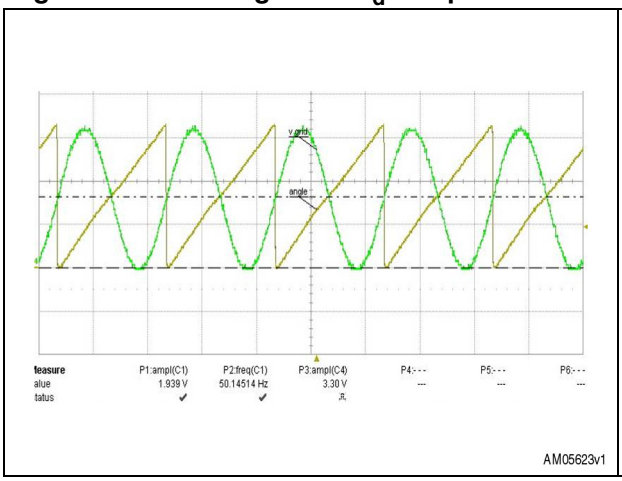


Figure 30. Grid angle and grid voltage

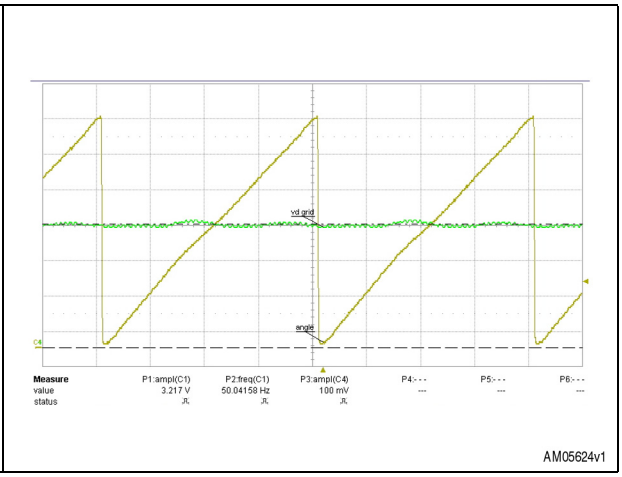
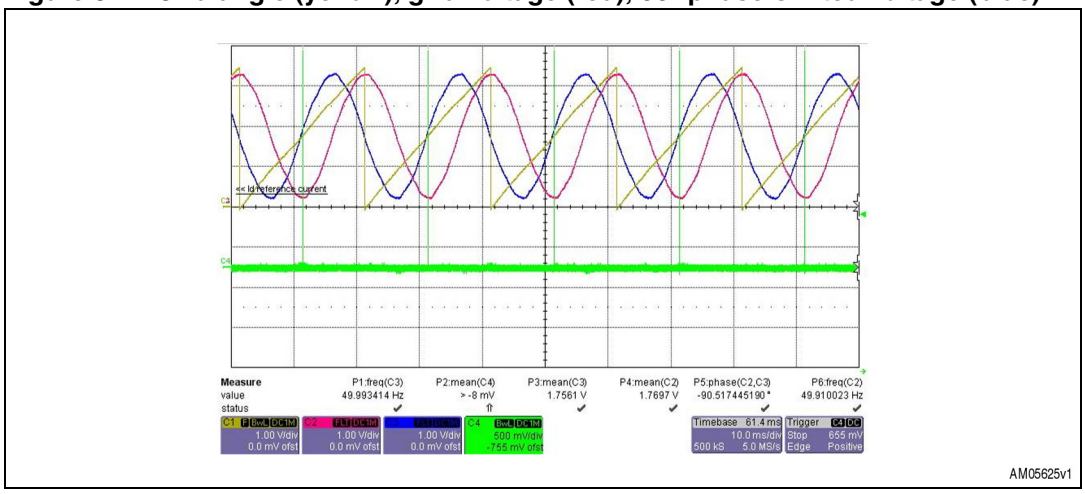


Figure 31. Grid angle (yellow), grid voltage (red), 90° phase-shifted voltage (blue)



The phase-shift modulation (*Figure 32*) for the DC-DC stage is also implemented in the digital control loop. The STM32F103xx microcontroller allows a high resolution phase shift (16 ns), thanks to 16-bit timers, with a consequent advantage in terms of output voltage regulation of the DC-DC converter. In *Figure 33*, the driving signals of M1 and M6 are drawn, together with the HF transformer current in CCM and the M1 drain current under ZVS operation. Commutation of the device M1 may be seen in *Figure 34*, where the control signal is shown together with the drain source voltage and drain current at 200 V and 5 A input. *Figure 35* shows phase-shift and control signals (Ch1, Ch2), transformer primary voltage (Ch3), and secondary voltage (Ch4).

Figure 32. DC-DC phase-shift modulation

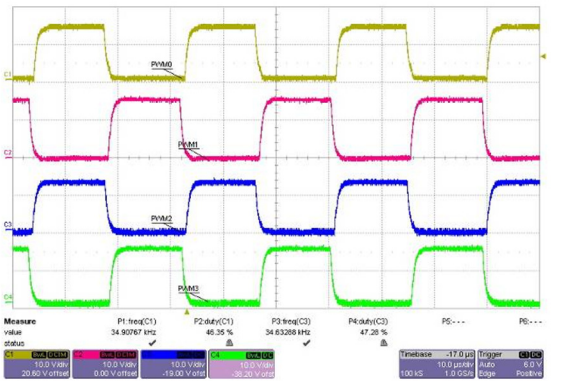


Figure 33. Phase-shifted signals, transformer current in CCM, power MOSFET M1 drain current

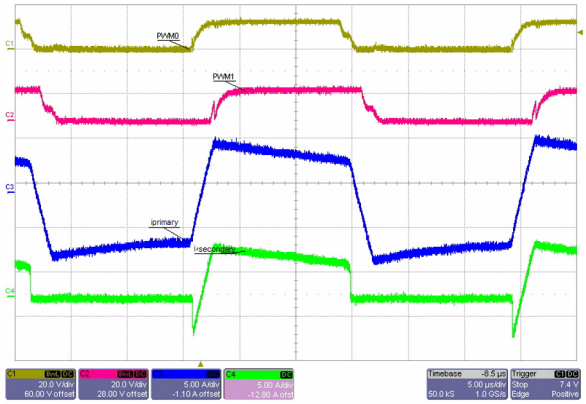


Figure 34. Power MOSFET M1- Ch1 gate signal; Ch2 drain-source voltage and drain current Ch4

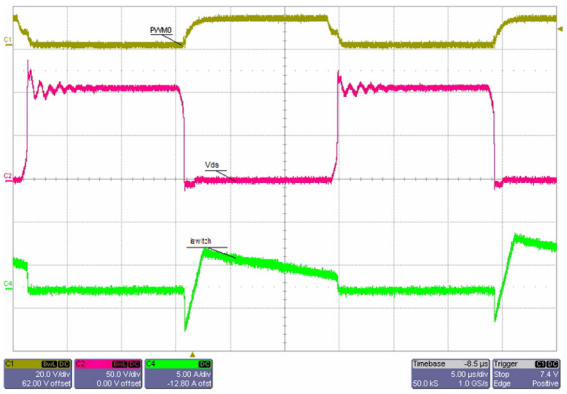
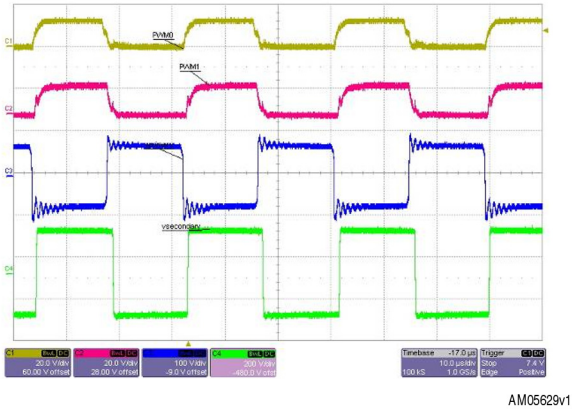


Figure 35. Phase-shifted gate signals (Ch1, Ch2), primary and secondary transformer voltage (Ch3, Ch4)



The PWM embedded peripheral used for the DC-AC stage is configured to generate a triangular carrier at 17.4 kHz with a resolution of 16,6 ns and programmable dead-time insertion to avoid cross-conduction. For the sake of security the complementary pairs must be disabled synchronously in the case of power stage failure/fault (e.g. overcurrent) and this is performed by a dedicated emergency stop input embedded in the peripheral.

Inverter output voltage and current are shown in *Figure 36*, *37*, *38* and *39* at different power levels and both in standalone and grid-connected operation. The efficiency of the DC-DC converter and overall system is shown in *Figure 40* and *41*, with different values of input voltage. Further improvements in terms of efficiency are possible using the hybrid inverter topology (two low frequency IGBTs and two high frequency MOSFETs). In this case the modulating strategy controlling the high-side devices (MOSFETs) and the low-side devices (IGBTs) must be modified according to the information in *Figure 42* and *43*, where the modulation used for the high-side and low-side devices is shown. The proposed converter performs with a power factor value higher than 90 % for any power level above 1 % of

nominal output power and current THD percentage slightly higher than 5 % at 2500 W output power, as measured in *Figure 44* and *45*.

Figure 36. DC-AC voltage and current in standalone mode (open-loop operation)

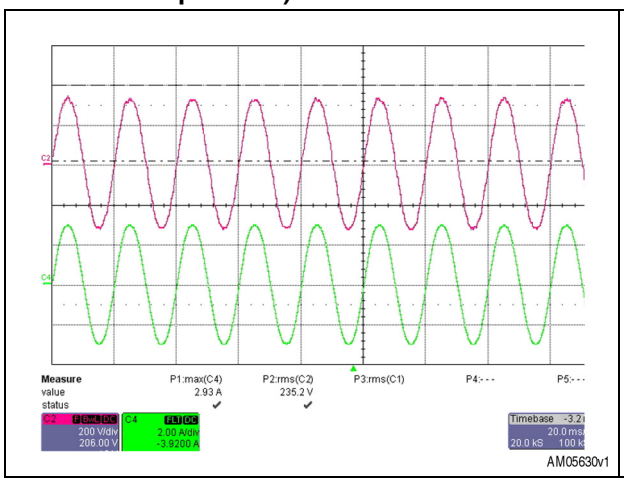


Figure 37. Grid voltage (blue), inverter voltage (red), injected current (green); injected power (math function)

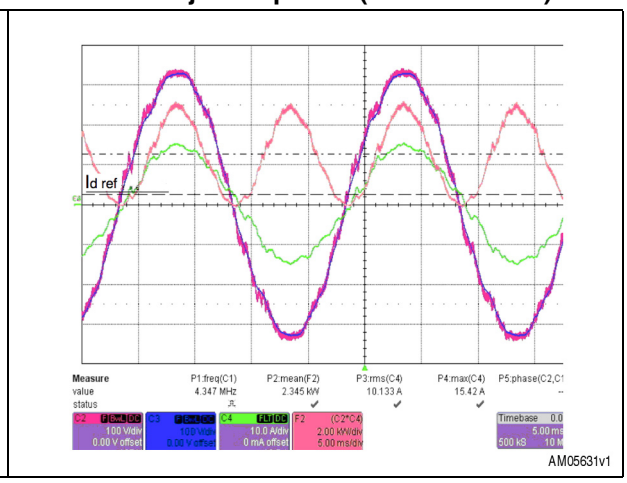


Figure 38. Inverter voltage (green) and current (blue) at 800 W,PF=0.97

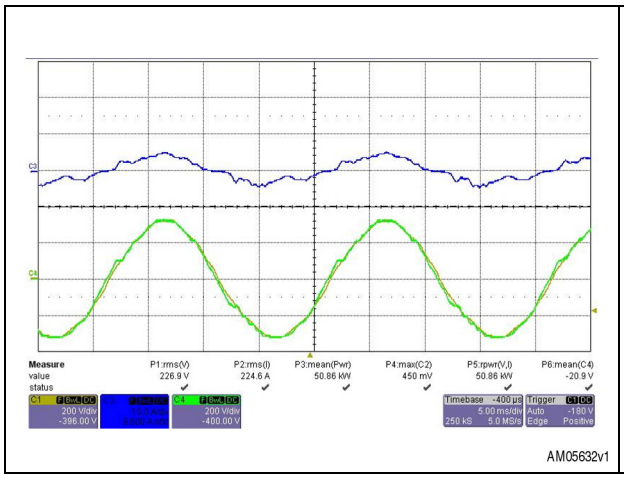


Figure 39. Inverter voltage (green) and current (yellow) at 2500 W, PF

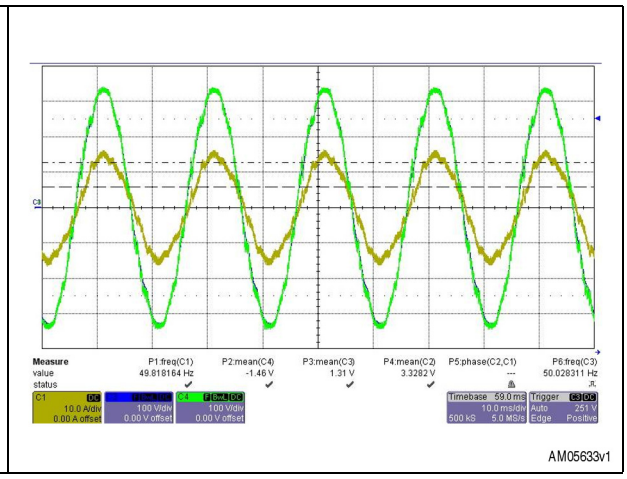


Figure 40. DC-DC converter efficiency at different input voltages

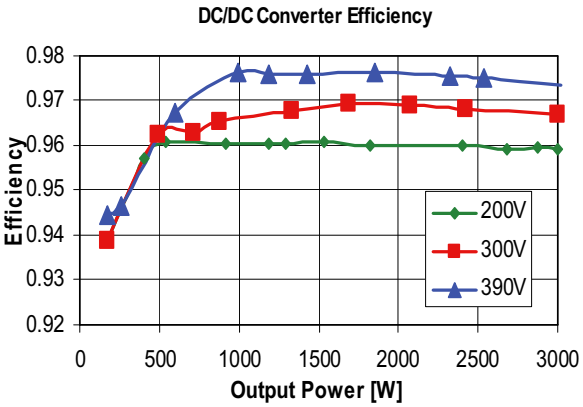


Figure 41. System efficiency

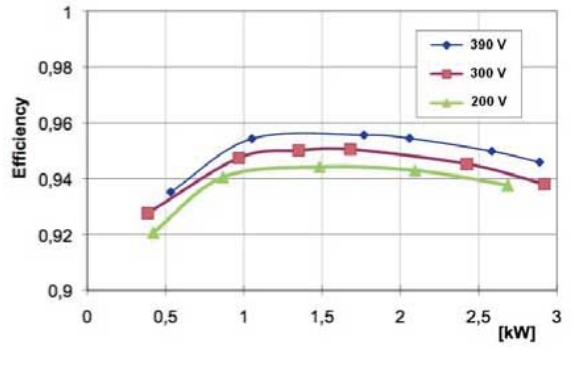


Figure 42. MOSFET M1- Ch1 gate signal, Ch2 drain-source voltage and Ch 4 drain current

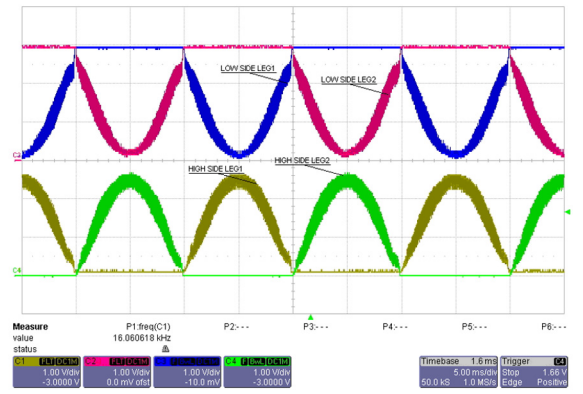


Figure 43. Phase-shifted gate signals (Ch1, Ch2), primary and secondary transformer voltage (Ch3, Ch4)

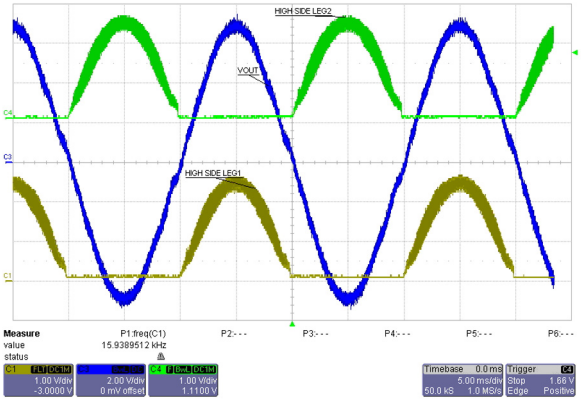


Figure 44. Low-side device modulation (red and blue track); high-side device modulation (yellow track and green track)

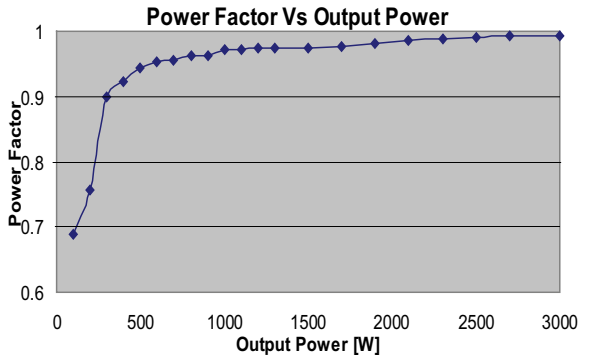
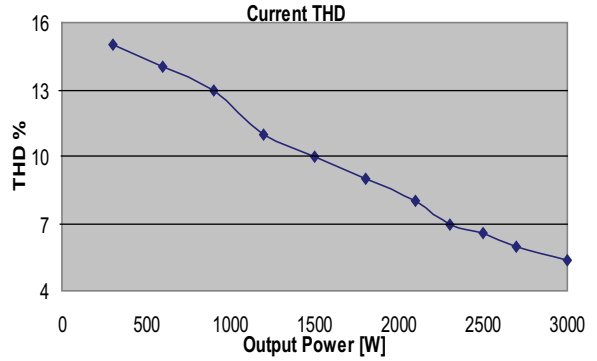


Figure 45. High-side device modulation in leg 1 (yellow track); high-side device modulation in leg 2 (green track); inverter output voltage (blue track)



8 Conclusions

This application note describes the design and performance of a power conversion architecture characterized by high efficiency, good integration levels and galvanic isolation, with the aim of demonstrating STMicroelectronics' complete and high performing product portfolio to implement any PV conversion system. For this reason, the power converter, based on a dual-stage topology, has been investigated and experimentally evaluated for photovoltaic applications. The converter performs MPPT and grid connection by means of an ARM Cortex M3-based STM32F103xx microcontroller, which is proven to be well suited for such an application. In fact, the implemented DQ axis control scheme shows excellent regulation of both active and reactive power, as is also required for low power applications in the near future. Simulation and experimental results have confirmed the consistency of the proposed solution for PV generation systems.

9 References

1. Review of PV Inverter Technology Cost and Performance Projections, 2006, NREL Report No. SR-620-38771
2. The 4th edition of Solar Generation - a publication in cooperation between The European Photovoltaic Industry Association and Greenpeace. September 2007
3. “A review of single-phase grid-connected inverters for photovoltaic modules”, IEEE Transactions on Industry Applications, vol. 41, n. 5, sept/oct. 2005, pp. 1292-1306
4. “Developing a 'next generation' PV inverter,” in Proc. 29th IEEE Photovolt. Spec. Conf., May 19-24, 2002, pp. 1352-1355
5. “A High Gain Transformer-Less DC-DC Converter for Fuel-Cell Applications”, 36th IEEE Power Electronics Specialists, Conference, 11-14 Sept. 2005, p. 2514 - 2520
6. “High-frequency link inverter for fuel cells based on multiple-carrier PWM”, IEEE Transactions on Power Electronics volume 19, issue 4, sept. 2004 pp:1279 - 1288
7. “Performance characterization of a high-power dual active bridge DC-to-DC converter”, IEEE Transactions on Industry Applications; volume 28, Issue 6, Nov.-Dec. 1992 pp:1294 - 130
8. “Comparison study of phase-shifted full bridge ZVS converters”, IEEE 35th Power Electronics Specialists Conference, 2004, PESC 04, volume 1, pp: 533 - 539. 20-25 June 2004
9. “Performance Optimization of a High Current Dual Active Bridge with a Wide Operating Voltage Range”, 37th IEEE Power Electronics Specialists Conference, PESC 06, 18-22 June 2006, pp:1-7
10. “Transformer-Coupled Multiport ZVS Bi-directional DC-DC Converter With Wide Input Range”, IEEE Transactions on Power Electronics, volume. 23, n. 2, March 2008, pp: 771 - 781
11. “A Three-phase Soft-switched High-power-density DC/DC Converter for High-power Applications”, IEEE Transactions on Industry Applications, volume 27, Issue 1, Jan.-Feb. 1991 pp. 63 - 73
12. “A single-stage three-phase grid-connected photovoltaic system with modified MPPT method and reactive power compensation,” IEEE Transaction on Energy Conversion, volume 22, Issue 4, Dec. 2007, pp. 881-886
13. “Intelligent PV module for grid-connected PV systems”, IEEE Transaction Industrial Electronics, vol. 53, Issue 4, Jun. 2006, pp: 1066-1073
14. “Photovoltaic power conditioning system with line connection”, IEEE Transaction on Industrial Electronics, vol. 53, no. 4, Jun. 2006, pp. 1048-1054
15. “Overview of control and grid synchronization for distributed power generation systems”, IEEE Transaction on Industrial Electronics, vol. 53, Issue 5, Oct. 2006, pp. 1398-1409
16. “Advanced grid synchronization system for power converters under unbalanced and distorted operating conditions”, in Proc. 32nd IEEE Annual Conference, IECON06, Nov. 2006, pp: 5173 - 5178
17. “Optimization of perturb and observe maximum power point tracking method”, IEEE Transactions on Power Electronics, vol. 20, no. 4, July 2005, pp. 963 - 973
18. “Comparison of photovoltaic array maximum power point tracking techniques”, IEEE Transaction on Energy Conversion, vol. 22, no. 2, Jun. 2007, pp. 439-449

19. “Analysis and Software Implementation of a Robust Synchronizing PLL Circuit Based on the pq Theory”, IEEE Transactions on Industrial Electronics, vol. 53, Issue 6, Dec. 2006, pp: 1919 - 1926
20. “Stability of Photovoltaic and wind turbine grid-connected inverters for a large set of grid impedance values”, IEEE Transactions on Power Electronics, vol. 21, n. 1, Jan 2006, pp. 263-272.

10 Revision history

Table 8. Document revision history

Date	Revision	Changes
02-Aug-2010	1	Initial release.
21-Jun-2011	2	Modified: *Figure 14* Added reference to the STEVAL-ISV002V2 demonstration board on coverpage.
08-Nov-2012	3	Modified: *Figure 22* and *23*